IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Cheng-Lien Chiang		
Assignee:	Bridge Semiconductor Corporation		
Title:	SEMICONDUCTOR PACKAGE DEVICE		
Serial No.:	10/042,812	Filed:	January 9, 2002
Examiner:	Chu. C.	Group Art Unit:	2815
Atty. Docket No.:	BDG005		

COMMISSIONER FOR PATENTS
P.O. Box 1450
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APPEAL BRIEF
(37 C.F.R. § 1.192)

Dear Sir:

This Appeal Brief is in furtherance of the Notice of Appeal filed concurrently herewith.

Applicant is a small entity. Please charge the $160 fee under 37 C.F.R. § 1.17(c) to Deposit Account No. 502178/BDG005 and charge any underpayment or credit any overpayment to this Account.

This paper is submitted in triplicate.

The index of subject matter is as follows:

I. REAL PARTY IN INTEREST

The real party in interest in this appeal is Bridge Semiconductor Corporation.

II. RELATED APPEALS AND INTERFERENCES

U.S. Application Serial No. 10/082,500 filed February 25, 2002 is a continuation-in-part of the captioned-application. An Appeal Brief for the '500 application was filed on August 18, 2003, and an Answer is due. *Nakamura et al.* (U.S. Patent No. 5,405,809) is cited in obviousness rejections in both the captioned-application and the '500 application. *Nakamura et al.* is a secondary reference in the captioned-application and a primary reference in the '500 application, and *Nakamura et al.* is combined with different references in the captioned-application and the '500 application. However, the question of whether removing light-transmitting substrate 1 (or light-transmitting substrate 21) from the semiconductor device (or image sensor device) in Fig. 1 (or Fig. 2) is a proper modification of *Nakamura et al.* arises in both appeals. In addition, the question of whether resin layer 8 (or transparent resin 28) is recessed relative to resin coating 7 (or resin coating 27) in Fig. 1 (or Fig. 2) of *Nakamura et al.* arises in both appeals. Therefore, the appeals for captioned-application and the '500 application affect one another.

There are no other appeals or interferences that will directly affect or be directly affected by or have a bearing on the Board's decision in this appeal.

III. STATUS OF CLAIMS

A. Total Number of Claims in Application

Claims in the application are: 1-120

B. Status of All Claims

1.	Claims canceled:	NONE
2.	Claims withdrawn:	NONE
3.	Claims pending:	1-120
4.	Claims allowed:	NONE
5.	Claims rejected:	1-120

C. Claims on Appeal

Claims on appeal are: 1-120

IV. STATUS OF AMENDMENTS

A Response has been filed after the outstanding Office Action dated August 15, 2003, that amends the Specification to improve clarity. The Specification amendments are unrelated to the issues on appeal.

V. SUMMARY OF INVENTION

The present invention is generally directed to a semiconductor package device (Specification, page 4, lines 2-3).

In accordance with one aspect of the invention, a semiconductor package device includes an insulative housing, a semiconductor chip, a terminal and a lead, wherein the insulative housing includes a top surface, a bottom surface, and a peripheral side surface between the top and bottom surfaces, the chip includes a conductive pad, the terminal protrudes downwardly from and extends through the bottom surface and is electrically connected to the pad, the lead protrudes laterally from and extends through the side surface and is electrically connected to the pad, the terminal and the lead are spaced and separated from one another outside the insulative housing, and the terminal and the lead are electrically connected to one another inside the insulative housing and outside the chip (Specification, page 4, lines 13-21).

An embodiment of the present invention discloses a semiconductor package device and its method of manufacture. The method includes providing semiconductor chip 110 that includes upper surface 112 and lower surface 114, where upper surface 112 includes conductive pads 116 (Specification, page 10, lines 5-10 and Figs. 1A and 1B), providing metal base 120 that includes surfaces 122 and 124, central portion 126, slots 128, recessed portions 130, 132 and 134, non-recessed portions 136 and leads 138, where recessed portions 130 are formed in surface 122 and spaced from slots 128, recessed portions 132 are formed in surface 124 between slots 128, non-recessed portions 136 are formed between slots 128, and leads 138 include recessed portions 132 and non-recessed portions 136 (Specification, page 10, line 30 to page 11, line 9 and Figs. 2A and 2B), forming metal traces 144 on metal base 120, where metal traces 144 include terminals 146 in recessed portions 130 and routing lines 148 outside recessed portions 130 that extend to recessed portions 132, and conductive traces 150 include leads 138 and metal traces 144 (Specification, page 13, lines 3-16 and Figs. 3A and 3B), forming adhesive 154 on metal base 120 and metal traces 144 (Specification, page 15, lines 1-2 and Figs. 4A and 4B), mechanically attaching chip 110 to metal base 120 using adhesive 154 (Specification, page 15, lines 17-18 and Figs. 5A and 5B), forming encapsulant 156 on chip 110 and metal base 120, where encapsulant

156 includes top surface 160, peripheral side surfaces 162, bottom surface 164 and peripheral portion 166 (Specification, page 16, lines 14-15 and page 17, lines 9-11 and Figs. 6A and 6B), removing encapsulant 156 from laterally extending portions of slots 128 (Specification, page 18, lines 3-4 and Figs. 7A and 7B), forming protective coating 170 on metal base 120 outside encapsulant 156 (Specification, page 18, lines 19-20 and Figs. 8A and 8B), removing central portion 126 of metal base 120, thereby exposing terminals 146, routing lines 148 and adhesive 154 (Specification, page 19, lines 17-18 and 22 and Figs. 9A and 9B), forming openings 176 in adhesive 154 that expose pads 116 (Specification, page 20, lines 20-22 and Figs. 10A and 10B), forming connection joints 180 in openings 176 that contact and electrically connect pads 116 and routing lines 148 (Specification, page 21, lines 9-10 and Figs. 11A and 11B), forming insulative base 182 on the structure, where terminals 146 are exposed, and encapsulant 156 and insulative base 182 in combination form insulative housing 184 that surrounds and encapsulates chip 110 (Specification, page 22, lines 15-16 and 26-27 and page 23, lines 2-4 and Figs. 12A and 12B), singulating semiconductor package device 186 from the lead frame (Specification, page 23, lines 16-22 and Figs. 13A and 13B), bending leads 138 (Specification, page 24, lines 7-8 and Figs. 14A and 14B), and trimming semiconductor package device 186 (Specification, page 26, lines 19-20 and Figs. 15A and 15B).

Device 186 as shown in Figs. 13A and 13B includes chip 110, conductive traces 150, adhesive 154, connection joints 180 and insulative housing 184. Conductive traces 150 each include a lead 138 that protrudes laterally from and extends through a side surface 162 of insulative housing 184, a terminal 146 that protrudes downwardly from and extends through bottom surface 164 of insulative housing 184, and a routing line 148 within insulative housing 184 that is integral with an associated terminal 146 and contacts an associated lead 138 and connection joint 180. Conductive traces 150 are electrically connected to pads 116 by connection joints 180 in one-to-one relation, and are electrically isolated from one another. Leads 138 are arranged in opposing rows that protrude laterally from and extend through opposing side surfaces 162 and are disposed between top surface 160 and bottom surface 164. Terminals 146 are arranged as an array that protrudes downwardly from and extends through bottom surface 164 and is disposed inside inner side surfaces 174. Furthermore, leads 138 and

terminals 146 are spaced and separated from one another outside insulative housing 184, and leads 138 and terminals 146 are electrically connected to one another and to pads 116 inside insulative housing 184 and outside chip 110. (Specification, page 23, line 23 to page 24, line 6.)

VI. ISSUES[1]

The issues on appeal are as follows:

1. Whether claims 1-20 are unpatentable under 35 U.S.C. § 103(a) over *Shin et al.* (U.S. Patent No. 5,866,939) in view of *Nakamura et al.* (U.S. Patent No. 5,405,809);

2. Whether claims 21-40 are unpatentable under 35 U.S.C. § 103(a) over *Shin et al.* in view of *Nakamura et al.*;

3. Whether claims 41, 45-51, 57-60, 101, 105-111 and 117-120 are unpatentable under 35 U.S.C. § 103(a) over *Shin et al.* in view of *Huang et al.* (U.S. Patent No. 6,198,171);

4. Whether claims 42-44, 52-56, 102-104 and 112-116 are unpatentable under 35 U.S.C. § 103(a) over *Shin et al.* in view of *Huang et al.* and *Nakamura et al.*;

5. Whether claims 61, 65, 66, 68-71 and 78-80 are unpatentable under 35 U.S.C. § 103(a) over *Osawa* (Japanese Patent Publication No. 06-097352) in view of *McShane et al.* (U.S. Patent No. 5,157,480);

6. Whether claims 62-64 are unpatentable under 35 U.S.C. § 103(a) over *Osawa* in view of *McShane et al.* and *Happ* (U.S. Patent No. 3,627,901);

7. Whether claims 72-76 are unpatentable under 35 U.S.C. § 103(a) over *Osawa* in view of *McShane et al.* and *Happ*;

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[1] Claims 1-40 are rejected under 35 U.S.C. § 103(a) as being unpatentable over *Shin et al.* in view of *Nakamura et al.* at Section 6 in the outstanding Office Action dated August 15, 2003. Section 6 sets forth separate basis for rejection for claims 1, 11, 21, and 31. Thus, the Examiner has set forth separate grounds of rejection for claims 1, 11, 21 and 31 that constitute separate issues for appeal.

Claims 1 and 11 are sufficiently similar that they have been consolidated into the first issue for appeal, and claims 21 and 31 are sufficiently similar that they have been consolidated into the second issue for appeal.

Claims 62-64, 72-76, 81-87, 89-97, 99 and 100 are rejected under 35 U.S.C. § 103(a) as being unpatentable over *Osawa* in view of *McShane et al.* and *Happ* at Section 10 in the outstanding Office Action dated August 15, 2003. Section 10 sets forth separate basis for rejection for claims 62, 72, 81 and 91. Thus, the Examiner has set forth separate grounds of rejection for claims 62, 72, 81 and 91 that constitute separate issues for appeal.

Claims 81 and 91 are sufficiently similar that they have been consolidated into the eighth issue for appeal.

8. Whether claims 81-87, 89-97, 99 and 100 are unpatentable under 35 U.S.C. § 103(a) over *Osawa* in view of *McShane et al.* and *Happ*;

9. Whether claims 67 and 77 are unpatentable under 35 U.S.C. § 103(a) over *Osawa* in view of *McShane et al.* and *Kimura* (U.S. Patent No. 6,218,728); and

10. Whether claims 88 and 98 are unpatentable under 35 U.S.C. § 103(a) over *Osawa* in view of *Happ*, *McShane et al.* and *Kimura*.

VII. GROUPING OF CLAIMS

For the first issue on appeal, the claims do not stand and fall together and are grouped as follows: (i) claims 1-6, 8-9, 11-16 and 19, (ii) claims 7 and 17, (iii) claims 10 and 20, and (iv) claim 18.

For the second issue on appeal, the claims do not stand and fall together and are grouped as follows: (i) claims 21-25 and 27-29, (ii) claims 26, 31-35 and 37-39, (iii) claim 30, (iv) claim 36, and (v) claim 40.

For the third issue on appeal, the claims do not stand and fall together and are grouped as follows: (i) claims 41, 45, 46, 48, 49, 101, 105, 108 and 109, (ii) claims 47 and 106, (iii) claims 50 and 110, (iv) claim 107, (v) claims 51, 59, 111 and 119, (vi) claims 57 and 117, (vii) claim 58, (viii) claims 60 and 120, and (ix) claim 118.

For the fourth issue on appeal, the claims do not stand and fall together and are grouped as follows: (i) claims 42-44 and 102-104, and (ii) claims 52-56 and 112-116.

For the fifth issue on appeal, the claims do not stand and fall together and are grouped as follows: (i) claims 71 and 78-80, and (ii) claims 61, 65, 66 and 68-70.

For the sixth issue on appeal, the claims do not stand and fall together and are grouped as follows: (i) claims 62 and 64, and (ii) claim 63.

For the seventh issue on appeal, the claims do not stand and fall together and are grouped as follows: (i) claims 72, 75 and 76, and (ii) claims 73 and 74.

For the eighth issue on appeal, the claims do not stand and fall together and are grouped as follows: (i) claims 81, 87, 89 and 90, (ii) claims 82 and 85, (iii) claims 83 and 84, (iv) claims 86, 91, 97, 99 and 100, (v) claims 92 and 95, (vi) claims 93 and 94, and (vii) claim 96.

For the ninth issue on appeal, the claims do not stand and fall together and are grouped as follows: (i) claim 77, and (ii) claim 67.

For the tenth issue on appeal, the claims do not stand and fall together and are grouped as follows: (i) claim 88, and (ii) claim 98.

VIII. ARGUMENTS

1. Section 103 Rejections – Claims 1-20

Claims 1-20 are rejected under 35 U.S.C. § 103(a) as being unpatentable over *Shin et al.* (U.S. Patent No. 5,866,939) in view of *Nakamura et al.* (U.S. Patent No. 5,405,809).

Shin et al.

Shin et al. addresses lead end grid array semiconductor package size reduction:

> However, such a conventional quad flat semiconductor package is difficult to reduce in size because the leads are in the same plane as the plastic encapsulating part and extend from the four sides of the package to the exterior. In addition, the high integration of semiconductor chips requires an exceptionally increased number of pins the distance between which has been technically difficult to narrow to a certain value. Thus, to accommodate a large number of pins, a large-sized package is necessary, which results in retrogradation against the tendency toward the small size of semiconductor packages. (Col. 1, lines 34-44.)

Shin et al. solves the problem by bending a lead frame so that the leads include a different plane direction-converting lead part, an identical plane direction-converting lead part, and a bending part therebetween. The leads ends are distributed as a grid array. Furthermore, the grid array is as small as or similar to the area of the semiconductor chip.

> Therefore, it is an objective of the present invention to provide a grid array type lead frame in which the package area is reduced similar to the size of a semiconductor chip while the exposed lead ends used as input and output ends are increased in the number per area, and a lead end grid array semiconductor package utilizing such a lead frame. (Col. 2, lines 41-46.)

> It is a further objective of the present invention to provide a grid array type lead frame in which the exposed lead ends with an increased number per area are farther distant from each other while the package area is reduced similar to the size of a semiconductor chip, and a lead end grid array semiconductor package utilizing such a lead frame. (Col. 2, lines 47-52.)

> More particularly, the present invention relates to a grid array type lead frame having a plurality of leads classified into groups by length, in each of which at least one different plane direction-converting lead part and/or at least one identical plane direction-converting lead part is formed by at least one bending part, thereby distributing leads ends in a grid array, and a lead end grid array semiconductor package employing the same, which is as small as or similar to that of a semiconductor chip in area . . . (Col. 1, lines 9-17.)

Shin et al. discloses grid array type lead frame 1 which includes leads 2 and chip pad 5.

Leads 2 include direction-converting lead parts 2a and 2b, first and second bending parts 3 and 3a, and lead ends 4. Direction-converting lead parts 2a and 2b are introduced into different planes by first and second bending parts 3 and 3a, respectively. Different plane direction-converting part 2a is slant bent to the XY axis and the XZ axis by first bending part 3, and different plane direction-converting part 2b is bent to the X axis and the Y axis by second bending part 3a.

Leads 2 are bent to the X axis and/or Y axis, and the Z axis, and extend to the same plane below the semiconductor chip mounting area where lead ends 4 form a grid array. Each lead end 4 includes lead prominence 4' used as an input and output terminal after completion of the semiconductor package fabrication.

A semiconductor chip is attached to chip pad 5 by an adhesive such as epoxy resin or tape. Thereafter, a liquid of encapsulating resin is molded into a plastic encapsulating part that surrounds the chip.

In Fig. 10A, lead end grid array semiconductor package 10α (mislabeled 10β) includes lead 2 extending to lead end 4 with prominence 4', semiconductor chip 20 mounted on chip pads 5' by an adhesive such as epoxy resin or tape, bond wire 30 that electrically connects lead 2 to chip 20, and plastic encapsulating part 40 that protects lead 2, chip 20 and bond wire 30 from the external environment. Lead end 4 protrudes from the bottom of plastic encapsulating part 40, and prominence 4' is an input and output terminal distributed in a grid array.

In Fig. 10B, lead end grid array semiconductor package 10β (mislabeled 10α) is a modified version of package 10α in which chip 20 is inverted and lead 2 is electrically connected to chip 20 by solder joint 31 rather than bond wire 30. Alternatively, lead 2 can be electrically connected to chip 20 by a bond wire.

Nakamura et al.

Nakamura et al. discloses a semiconductor device that includes light-transmitting substrate 1, circuit conductor layer 2, plated metal layer 3, metal bump 4, semiconductor chip 6, resin coating 7 and resin layer 8. Semiconductor chip 6 includes electrode 5.

Metal bump 4 is a metal such as Au that is formed on electrode 5 by plating or ball bonding, and then semiconductor chip 6 is cut out from a silicon wafer.

Circuit conductor layer 2 is a metal such as Cu or Al that is formed on light-transmitting substrate 1. For instance, circuit conductor layer 2 may be formed by depositing a metal layer on light-transmitting substrate 1 by sputtering, vapor deposition and the like and then patterning the metal layer using photolithography. Alternatively, circuit conductive layer 2 may be formed by attaching a flexible printed wiring board to light-transmitting substrate 1 or by thick-film printing.

Plated metal layer 3 is then formed on a prescribed portion of circuit conductor layer 2.

Resin layer 8 is then applied to a prescribed portion of light-transmitting substrate 1, and then semiconductor chip 6 is disposed face-down on resin layer 8 so that plated metal layer 3 abuts electrode 5. While semiconductor chip 6 is pressed onto light-transmitting substrate 1, resin layer 8 is irradiated with ultra violet rays through light-transmitting substrate 1 and partially cured.

The structure is then placed in an oven that melts plated metal layer 3 and further cures resin layer 8. Plated metal layer 3 melts and recoagulates so that alloy layers are formed in abutting portions between circuit conductor layer 2 and plated metal layer 3, and in abutting portions between plated metal layer 3 and metal bump 4.

Finally, resin coating 7 such as silicon is dispensed on light-transmitting substrate 1 and semiconductor chip 6.

Nakamura et al. emphasizes the importance of fully curing resin layer 8 to provide a strong physical connection between light-transmitting substrate 1 and semiconductor chip 6 so that the package is reliable and has good physical endurance:

> As is described above, in the first conventional method, the photo-curable insulating resin is cured by being irradiated with ultra violet rays through the transparent substrate. Therefore, a portion of the photo-curable insulating resin which is shaded by the circuit conductor layer formed on the transparent substrate may not be sufficiently irradiated with the ultra violet rays, and therefore may not be cured completely. In such cases, since the photocurable insulating resin is not completely cured, the physical connection between the semiconductor chip and the substrate is insufficient, causing the device to have poorer physical endurance. (Col. 2, lines 10-21.) (Emphasis added.)
>
> Moreover, the semiconductor device and the image sensor device each can be firmly mounted on a light-transmitting substrate, since a photo-thermal cross-linkable insulating resin included therein is completely cured through first and second curing steps, greatly improving the mounting yield of the devices. (Col. 5, lines 41-47.) (Col. 12, lines 55-61.) (Emphasis added.)
>
> Thus, the invention described herein makes possible the advantages of (1) providing a semiconductor device and an image sensor having high reliability, in which an insulating resin is completely cured and electrodes of a semiconductor chip have a firm electrical connection with a circuit conductor layer formed on a substrate, and (2) providing methods for producing such a semiconductor device and an image sensor device. (Col. 5, lines 51-59.) (Emphasis added.)

Accordingly, light-transmitting substrate 1 is an essential, permanent part of the semiconductor device, and semiconductor chip 6 is firmly mounted on light-transmitting substrate 1 by resin layer 8 to assure a high reliability device with good physical endurance.

Claims 1-6, 8-9, 11-16 and 19 (Group I)

Claim 1 recites "an insulative housing with a top surface, a bottom surface, and a peripheral side surface between the top and bottom surfaces, wherein the insulative housing includes a first single-piece housing portion and a second single-piece housing portion" and "the first single-piece housing portion contacts the lead and is spaced from the terminal, the second single-piece housing portion contacts the first single-piece housing portion and the terminal." Claim 11 recites similar limitations.

Shin et al. fails to teach or suggest this approach. Plastic encapsulating part 40 does not include a first single-piece housing portion that contacts lead 2 and is spaced from lead end 4 and a second single-piece housing portion that contacts the first single-piece housing portion and lead end 4. Instead, plastic encapsulating part 40 is a single-piece that contacts lead 2 and lead end 4. *Nakamura et al.* fails to cure this deficiency. There is no teaching, suggestion or motivation to modify *Shin et al.* using the assembly technique taught by *Nakamura et al.*, particularly since the proposed modification would render *Shin et al.* unsatisfactory for its intended purpose.

In sustaining this rejection, the Examiner states as follows:

> Regarding claim 1, Shin et al. discloses in Fig. 1A, Fig. 1B, Fig. 10B and column 6, lines 36 ~ 40 a semiconductor package device, comprising:
> - an insulative housing (40) with a top surface, a bottom surface, and a peripheral side surface between the top and bottom surfaces;
> - a semiconductor chip (20) within the insulative housing, wherein the chip includes an upper surface and a lower surface, and the upper surface includes a conductive pad (31);
> - a terminal (4 and 4') that protrudes downwardly from and extends through the bottom surface and is electrically connected to the pad; and
> - a lead (2) that protrudes laterally from and extends through the side surface and is electrically connected to the pad,
> - wherein the terminal and the lead are spaced and separated from one another outside the insulative housing, and the terminal and the lead are electrically connected to one another inside the insulative housing and outside the chip.

> Shin et al. does not disclose the insulative housing including a first single-piece housing portion and a second single-piece housing portion and the first single-piece housing portion contacting the lead and being spaced from the terminal, the second single-piece housing portion contacting the first single-piece housing portion and the terminal. However, Nakamura et al. teaches in Fig. 1 an insulative housing (7 and 8) including a first single-piece housing portion (7) and a second single-piece housing portion (8) and the first single-piece housing portion (7) contacting a lead (2) and being spaced from a terminal (4), the second single-piece housing portion (8) contacting the first single-piece housing portion and the terminal. Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Shin et al. by using the first and second single-piece housing portion for the insulative housing as taught by Nakamura et al. The ordinary artisan would have been motivated to modify Shin et al. in the manner described above for at least the purpose of providing a firm electrical connection with a circuit conductor layer formed on a substrate in a semiconductor device (column 5, lines 55 ~ 57).

The rejection is flawed for several reasons.

The proposed modification, as best Applicant can tell, is to use resin coating 7 and resin layer 8 in *Nakamura et al.* as plastic encapsulating part 40 in *Shin et al.*

The proposed modification is not taught or suggested by *Nakamura et al.*, has no motivation and would render *Shin et al.* unsatisfactory for its intended purpose, and fails to meet the claim limitations.

Nakamura et al. fails to teach or suggest the proposed modification. *Nakamura et al.* fails to teach or suggest bending circuit conductor layer 2 (like lead 2) such that only a small distal portion (like lead end 4) contacts light-transmitting substrate 1. Instead, the entire back side of circuit conductor layer 2 is mounted on and supported by light-transmitting substrate 1. *Nakamura et al.* also fails to teach or suggest exposing circuit conductor layer 2 at the bottom surface (like lead 2). Instead, light-transmitting substrate 1 is an essential, permanent part of the semiconductor device. Thus, *Nakamura et al.* fails to teach or suggest using resin coating 7 and resin layer 8 with a bent circuit conductor layer 2 (like lead 2) that must be exposed at the bottom surface (like lead 2).

The proposed modification would render *Shin et al.* unsatisfactory for its intended purpose. If *Shin et al.* were assembled in this manner then lead end 4 would contact light-transmitting substrate 1 on the side opposite the bottom surface. That is, light-transmitting substrate 1 would prevent lead end 4 from extending to or being exposed at the bottom surface. Instead, lead end 4 would be buried beneath light-transmitting substrate 1. *Shin et al.* provides a lead end grid array semiconductor package. The proposed modification would encapsulate the lead end grid array, thereby rendering *Shin et al.* unsatisfactory for its intended purpose.

The Examiner attempts to cure this fundamental deficiency by asserting that *Nakamura et al.* supplies the necessary motivation by providing a firm electrical connection with a circuit conductor layer formed on a substrate in a semiconductor device. However, *Nakamura et al.* provides the firm connection not only between the circuit conductor layer and the chip, but also between the light-transmitting substrate and the chip. *Nakamura et al.* emphasizes the importance of fully curing resin layer 8 to provide a strong physical connection between light-transmitting substrate 1 and semiconductor chip 6 so that the package is reliable and has good physical endurance. Thus, light-transmitting substrate 1 is an essential, permanent part of the semiconductor device. Since light-transmitting substrate 1 would cover lead end 4 and render *Shin et al.* unsatisfactory for its intended purpose, there is no motivation to do so.

The proposed modification fails to meet the claim limitations. Claim 1 recites "a terminal that protrudes downwardly from and extends through the bottom surface." Claim 11 recites similar limitations. *Shin et al.* fails to teach or suggest this approach if plastic encapsulating part 40 is replaced by resin coating 7 and resin layer 8. Instead, lead end 4 would be aligned with rather than protrude from resin layer 8. In sustaining this rejection, the Examiner asserts that "a terminal (4 and 4') that protrudes downwardly from and extends through the bottom surface." This is clearly erroneous under the proposed modification. Claim 1 also recites "a lead that protrudes laterally from and extends through the side surface." Claim 11 recites similar limitations. *Shin et al.* fails to teach or suggest this approach in Fig. 10B. Instead, lead 2 is aligned with the side surface of plastic encapsulating part 40. In sustaining this rejection, the Examiner asserts that "a lead (2) that protrudes laterally from and extends through the side surface." This is clearly erroneous.

Therefore, the proposed modification is clearly erroneous.

Claims 7 and 17 (Group II)

Claim 7 distinguishes over *Shin et al.* in view of *Nakamura et al.* for the reasons set forth above for the Group I claims and further distinguishes over *Shin et al.* in view of *Nakamura et al.* on its own merits since it recites another limitation that is not disclosed by *Shin et al.* in view of *Nakamura et al.*

Claim 7 recites "the lead is outside the periphery of the chip." Claim 17 recites similar limitations. *Shin et al.* fails to teach or suggest that lead 2 is outside the periphery of chip 20 in Fig. 10B. Instead, lead 2 extends within the periphery of chip 20 in Fig. 10B. In sustaining this rejection, the Examiner asserts that "Shin et al. discloses in Fig. 1A, Fig. 1B and Fig. 10B . . . the lead being outside the periphery of the chip." This is clearly erroneous.

Claims 10 and 20 (Group III)

Claim 10 distinguishes over *Shin et al.* in view of *Nakamura et al.* for the reasons set forth above for the Group I claims and further distinguishes over *Shin et al.* in view of *Nakamura et al.* on its own merits since it recites another limitation that is not disclosed by *Shin et al.* in view of *Nakamura et al.*

Claim 10 recites "the device is devoid of wire bonds, TAB leads and solder joints." Claim 20 recites similar limitations. *Shin et al.* fails to teach or suggest that package 10β is devoid of wire bonds, TAB leads and solder joints. Instead, lead 2 is electrically connected to chip 20 by bond wire 30 or solder joint 31. In sustaining this rejection, the Examiner asserts that "Shin et al. discloses in Fig. 1A, Fig. 1B and Fig. 10B the device being devoid of wire bonds, TAB lead and solder joints. . . Shin et al. discloses in column 16, line 43 the element 31 being a bump." This is clearly erroneous. *Shin et al.* discloses "bumps or solder joints 31" (col. 15, line 21) but fails to describe the bump composition. Those skilled in the art would likely infer that "bump" is shorthand for "solder bump" as is conventional with flip-chip bonding.

Claim 18 (Group IV)

Claim 18 distinguishes over *Shin et al.* in view of *Nakamura et al.* for the reasons set forth above for the Group I claims and further distinguishes over *Shin et al.* in view of *Nakamura et al.* on its own merits since it recites another limitation that is not disclosed by *Shin et al.* in view of *Nakamura et al.*

Claim 18 recites "the terminal is integral with a routing line that is plated on the lead inside the insulative housing, outside a periphery of the terminal and outside a periphery of the chip." *Shin et al.* fails to teach or suggest that lead end 4 is integral with a first portion of lead 2 that is plated on a second portion of lead 2 inside plastic encapsulating part 40 and outside the periphery of chip 20. Instead, lead 2 is a single continuous copper trace where it extends outside the periphery of chip 20. In sustaining this rejection, the Examiner asserts that "Shin et al. discloses in Fig. 10B and column 21, lines 22 ~ 28 the terminal being integral with a routing line that is plated on the lead inside the insulative housing, outside a periphery of the terminal and outside the periphery of the chip." This is clearly erroneous.

Shin et al. describes the plating as follows:

> It is preferred that the sites of the leads which are electrically connected to the bond pads for signal input and output by connection means, such as bumps or bond wires, are coated with silver or platinum to reduce electrical resistance, in the lead end grid array semiconductor packages 10α, 10β, 10, 10', 10", 10a–10j. The surfaces of the lead ends used as pins for signal input and output in the semiconductor package mounted on a mother board, are also preferred to be coated with platinum or palladium for the same reason as well as for the reason of high connection strength. (Col. 21, lines 22-31.)

Thus, *Shin et al.* discloses spot-plating lead 2 at (1) the site where bond wire 30 or solder joint 31 will contact it, and (2) lead end 4. *Shin et al.* fails to teach or suggest plating a portion of lead 2 that is integral with lead end 4 on another portion of lead 2 inside plastic encapsulating part 40 and outside the periphery of chip 20.

2. Section 103 Rejections – Claims 21-40

Claims 21-40 are rejected under 35 U.S.C. § 103(a) as being unpatentable over *Shin et al.* in view of *Nakamura et al.*

Claims 21-25 and 27-29 (Group I)

Claim 21 recites "an insulative housing with a top surface, a bottom surface, and peripheral side surfaces between the top and bottom surfaces, wherein the bottom surface includes a peripheral portion adjacent to the side surfaces and a central portion within the peripheral portion and spaced from the side surfaces, and the peripheral portion protrudes downwardly from the central portion."

Shin et al. fails to teach or suggest this approach. Plastic encapsulating part 40 does not include a peripheral portion that protrudes downwardly from a central portion. Instead, plastic encapsulating part 40 has a flat bottom surface. *Nakamura et al.* fails to cure this deficiency. There is no teaching, suggestion or motivation to modify *Shin et al.* using the assembly technique taught by *Nakamura et al.*, particularly since the proposed modification would render *Shin et al.* unsatisfactory for its intended purpose.

In sustaining this rejection, the Examiner states as follows:

> Regarding claim 21, Shin et al. discloses in Fig. 1A, Fig. 1B, Fig. 10B, Fig. 14 and column 6, lines 36 ~ 40 a semiconductor package device, comprising:
> - an insulative housing (40) with a top surface, a bottom surface, and peripheral side surfaces between the top and bottom surfaces;
> - a semiconductor chip (20) within and surrounded by the insulative housing, wherein the chip includes an upper surface and a lower surface, and the upper surface includes a conductive pad;
> - a terminal (4 and 4') that protrudes downwardly from and extends through a central portion of the bottom surface and is spaced from the side surfaces and is electrically connected to the pad; and
> - a lead (2) that protrudes laterally from and extends through

one of the side surfaces and is electrically connected to the pad,

- wherein the terminal and the lead are spaced and separated from one another outside the insulative housing, and the terminal and the lead are electrically connected to one another inside the insulative housing and outside the chip.

Shin et al. does not disclosure the bottom surface including a peripheral portion adjacent to the side surfaces and a central portion within the peripheral portion and spaced from the side surfaces, and the peripheral portion protrudes downwardly from the central portion. However, Nakamura et al. discloses in Fig. 1 a bottom surface (A) including a peripheral portion (B) adjacent to the side surfaces and a central portion (area of 8) within the peripheral portion and spaced from the side surfaces, and the peripheral portion protruding downwardly from the central portion. Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Shin et al. by using the peripheral portion as taught by Nakamura et al. The ordinary artisan would have been motivated to modify Shin et al. in the manner described above for at least the purpose of providing a firm electrical connection with a circuit conductor layer formed on a substrate in a semiconductor device (column 5, lines 55 ~ 57).

The rejection is flawed for several reasons.

The proposed modification is vague and confusing. The proposed modification, as best Applicant can tell, is to use resin coating 7 and resin layer 8 in *Nakamura et al.* as plastic encapsulating part 40 in *Shin et al.* However, it is unclear whether the proposed modification is to package 10β in Fig. 10B or package 10c in Fig. 14. Applicant should be given a reasonable explanation of what the proposed modification is rather than be forced to second-guess what it is. For this reason alone, the rejection is improper and should be overturned.

The proposed modification is not taught or suggested by *Nakamura et al.*, has no motivation and would render *Shin et al.* unsatisfactory for its intended purpose, and fails to meet the claim limitations.

Nakamura et al. fails to teach or suggest the proposed modification, as mentioned above for claim 1.

The proposed modification has no motivation and would render *Shin et al.* unsatisfactory for its intended purpose, as mentioned above for claim 1.

The proposed modification fails to meet the claim limitations.

Claim 21 recites "a terminal that protrudes downwardly from and extends through the central portion of the bottom surface." *Shin et al.* fails to teach or suggest this approach if plastic encapsulating part 40 is replaced by resin coating 7 and resin layer 8, as mentioned above for claim 1.

Claim 21 also recites "a lead that protrudes laterally from and extends through one of the side surfaces." *Shin et al.* fails to teach or suggest this approach, as mentioned above for claim 1.

Claim 21 also recites "the peripheral portion protrudes downwardly from the central portion." *Nakamura et al.* fails to teach or suggest that resin coating 7 protrudes downwardly from resin layer 8. Instead, resin coating 7 and resin layer 8 are aligned with one another and bounded by light-transmitting substrate 1. In sustaining this rejection, the Examiner asserts that "bottom surface (A) including peripheral portion (B)" of resin coating 7 protrudes downwardly from "central portion (area of 8)" of resin layer 8. This is clearly erroneous. Resin layer 8, where labeled in Fig. 1, extends to "bottom surface (A)."

Therefore, the proposed modification is clearly erroneous.

Claims 26, 31-35 and 37-39 (Group II)

Claim 26 distinguishes over *Shin et al.* in view of *Nakamura et al.* for the reasons set forth above for the Group I claims and further distinguishes over *Shin et al.* in view of *Nakamura et al.* on its own merits since it recites another limitation that is not disclosed by *Shin et al.* in view of *Nakamura et al.*

Claim 26 recites "the peripheral portion of the bottom surface protrudes a first distance below the central portion of the bottom surface, the terminal protrudes a second distance below the central portion of the bottom surface, and the first distance is greater than the second

distance." Claim 31 recites similar limitations. *Nakamura et al.* fails to teach or suggest that resin coating 7 protrudes downwardly from resin layer 8, much less that circuit conductor layer 2 protrudes downwardly from resin layer 8, much less that resin coating 7 protrudes downwardly from resin layer 8 a greater distance than circuit conductor layer 2 protrudes downwardly from resin layer 8. Instead, circuit conductor layer 2, resin coating 7 and resin layer 8 are aligned with one another and bounded by light-transmitting substrate 1. In sustaining this rejection, the Examiner asserts that "Nakamura et al. discloses in Fig. 1 the peripheral portion of the bottom surface protruding a first distance below the central portion of the bottom surface, the terminal protruding a second distance below the central portion of the bottom surface, and the first distance being greater than the second distance." This is clearly erroneous.

Claim 30 (Group III)

Claim 30 distinguishes over *Shin et al.* in view of *Nakamura et al.* for the reasons set forth above for the Group I claims and further distinguishes over *Shin et al.* in view of *Nakamura et al.* on its own merits since it recites another limitation that is not disclosed by *Shin et al.* in view of *Nakamura et al.*

Claim 30 recites "the device is devoid of wire bonds, TAB leads and solder joints." *Shin et al.* fails to teach or suggest this approach, as mentioned above for claim 10.

Claim 36 (Group IV)

Claim 36 distinguishes over *Shin et al.* in view of *Nakamura et al.* for the reasons set forth above for the Group II claims and further distinguishes over *Shin et al.* in view of *Nakamura et al.* on its own merits since it recites another limitation that is not disclosed by *Shin et al.* in view of *Nakamura et al.*

Claim 36 recites "wherein the first distance is about twice the second distance." *Nakamura et al.* fails to teach or suggest this approach, as mentioned above for claim 26. In sustaining this rejection, the Examiner asserts that "Nakamura et al. discloses in Fig. 1 the first distance being about twice the second distance." This is clearly erroneous.

Claim 40 (Group V)

Claim 40 distinguishes over *Shin et al.* in view of *Nakamura et al.* for the reasons set forth above for the Group II claims and further distinguishes over *Shin et al.* in view of *Nakamura et al.* on its own merits since it recites another limitation that is not disclosed by *Shin et al.* in view of *Nakamura et al.*

Claim 40 recites "the device is devoid of wire bonds, TAB leads and solder joints." *Shin et al.* fails to teach or suggest this approach, as mentioned above for claim 10.

3. Section 103 Rejections – Claims 41, 45-51, 57-60, 101, 105-111 and 117-120

Claims 41, 45-51, 57-60, 101, 105-111 and 117-120 are rejected under 35 U.S.C. § 103(a) as being unpatentable over *Shin et al.* in view of *Huang et al.* (U.S. Patent No. 6,198,171).

Huang et al.

Huang et al. addresses wire bond exposure and heat dissipation in a quad flat non-lead package:

> However, because of the demand for diminishing the thickness of the package, this conventional package structure is apt to expose the bonding wire 114 while encapsulating, thereby, the yield of the product become lower. Additionally, as the operating speed of the device of the integrated circuit becomes faster and faster nowadays. the heat generated increases accordingly, and since the conventional package structure is unable to provide a better way of heat dissipation, the performance of the electronic device will be affected. (Col. 1, line 64 to col. 2, line 6.)

Huang et al. solves the wire bond exposure problem by providing the lead with a stepped structure with a relatively thin portion to form a wire-bonding protruded zone, and improves heat dissipation by exposing the die pad.

> Therefore, it is the first objective of the present invention to provide a thermally enhanced quad flat non-lead package to improve the heat-dissipating effect of the package. (Col. 2, lines 8-10.)
>
> It is the second objective of the present invention to provide a thermally enhanced quad flat non-lead package capable of raising the yield. (Col. 2, lines 11-13.)
>
> The leads are disposed at the periphery of the die pad wherein the bottom surface of the lead has a stepped structure with a relatively thin portion to form a wire-bonding protruded zone. . . . The molding compound encapsulates the chip, bonding wires, the die pad, and a portion of the surface of the leads, but exposes the bottom surface of the die pad. (Col. 2, lines 24-32.)

Huang et al. discloses thermally enhanced quad non-lead package structure 220 that includes die pad 200, lead 202, chip 208, adhesive 214, bonding wire 216 and molding compound 218.

Die pad 200 is exposed to enhance the heat-dissipating effect.

Lead 202 includes first surface 206a and second surface 206b, and second surface 206b is a stepped structure formed with relatively thin wire-bonding protruded zone 226. As a result, bonding wire 216 is provided with accommodating space to assure that it is not exposed, thereby increasing product yield.

Claims 41, 45, 46, 48, 49, 101, 105, 108 and 109 (Group I)

Claim 41 recites "a lead that protrudes laterally from and extends through the side surface and is electrically connected to the pad, wherein the lead includes a recessed portion that contacts and extends into the insulative housing and is spaced from the top and bottom surfaces and does not overlap the chip and a non-recessed portion that contacts and extends outside the insulative housing and is adjacent to the recessed portion and the bottom surface." Claim 101 recites similar limitations.

Shin et al. fails to teach or suggest this approach. Lead 2 does not include a recessed portion that contacts and extends into plastic encapsulating part 40 and is spaced from the top and bottom surfaces and does not overlap the chip and is adjacent to a non-recessed portion that contacts and extends outside plastic encapsulating part 40 and is adjacent to the bottom surface, is spaced and separated from lead end 4 outside plastic encapsulating part 40, and is electrically connected to lead end 4 inside plastic encapsulating part 40 and outside chip 20. Instead, lead 2 has uniform thickness inside plastic encapsulating part 40 and outside chip 20. *Huang et al.* fails to cure this deficiency. There is no teaching, suggestion or motivation to modify *Shin et al.* using the assembly technique taught by *Huang et al.*, particularly since the proposed modification would render *Shin et al.* unsatisfactory for its intended purpose.

In sustaining this rejection, the Examiner states as follows:

> Regarding claim 41, Shin et al. discloses in Fig. 1A, Fig. 1B, Fig. 10B, Fig. 14 and column 6, lines 36 ~ 40 a semiconductor package device, comprising:
> - an insulative housing (40) with a top surface, a bottom surface, and a peripheral side surface between the top and bottom surfaces;
> - a semiconductor chip (20) within the insulative housing, wherein the chip includes an upper surface and a lower surface, and the upper surface includes a conductive pad;
> - a terminal (4) that protrudes downwardly from and extends through the bottom surface and is electrically connected to the pad; and
> - a lead (2) that protrudes laterally from and extends through the side surface and is electrically connected to the pad,
> - wherein the terminal and the lead are spaced and separated from one another outside the insulative housing, and the terminal and the lead are electrically connected to one another inside the insulative housing and outside the chip.
>
> Shin et al. does not disclose the lead includes a recessed portion. However, Huang et al. discloses in Fig. 3 a lead (202) including a recessed portion (226) that contacts and extends into the insulative housing (218) and is spaced from top and bottom surfaces and does not overlap a chip (208) and a non-recessed portion (an area of 206b) that contacts and extends outside the insulative

> housing (218) and is adjacent to the recessed portion and the bottom surface. Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Shin et al. by using the peripheral portion as taught by Huang et al. The ordinary artisan would have been motivated to modify Shin et al. in the manner described above for at least the purpose of increasing the encapsulating area of the molding compound on the surface of the lead (column 4, lines 20 ~ 24).

The rejection is flawed for several reasons.

The proposed modification is vague and confusing. The proposed modification, as best Applicant can tell, is to form wire-bonding protruded zone 226 in *Huang et al.* in lead 2 in *Shin et al.* However, it is unclear what the "peripheral portion" is. *Huang et al.* fails to mention a peripheral portion, and the Examiner's depiction of *Huang et al.* fails to mention a peripheral portion. Furthermore, it is unclear whether the proposed modification is to package 10β in Fig. 10B or package 10c in Fig. 14. Applicant should be given a reasonable explanation of what the proposed modification is rather than be forced to second-guess what it is. For this reason alone, the rejection is improper and should be overturned.

The proposed modification is not taught or suggested by *Huang et al.*, has no motivation and would render *Shin et al.* unsatisfactory for its intended purpose, and fails to meet the claim limitations.

Huang et al. fails to teach or suggest the proposed modification. *Huang et al.* fails to teach or suggest that lead 202 overlaps chip 208 (like lead 2 overlaps chip 20). Instead, die pad 200 overlaps chip 208 and lead 202 does not overlap chip 208. *Huang et al.* also fails to teach or suggest that wire-bonding protruded zone 226 faces towards chip 208 (as a wire-bonding protruded zone of lead 2 would face towards chip 20). Instead, wire-bonding protruded zone 226 faces away from chip 208. *Huang et al.* also fails to teach or suggest that wire-bonding protruded zone 226 is an intermediate portion of lead 202 (as a wire-bonding protruded zone of lead 2 would be due to lead end 4). Instead, wire-bonding protruded zone 226 is a distal end of lead 202. *Huang et al.* also fails to teach or suggest that wire-bonding protruded zone 226 is formed where lead 202 would otherwise be covered by molding compound 218 (as lead 2 would

be covered by plastic encapsulating part 40). Instead, wire-bonding protruded zone 226 is formed where lead 202 would otherwise be exposed. *Huang et al.* also fails to teach or suggest that lead 202 can be used in a lead end grid array semiconductor package where the grid array is as small as or similar to the area of the semiconductor chip (like packages 10β and 10c). Instead, lead 202 is used in a thermally enhanced quad non-lead package structure in which die pad 200 overlaps most of chip 208 and lead 202 overlaps none of chip 208. Thus, *Huang et al.* fails to teach or suggest using wire-bonding protruded zone 226 in lead 2.

The proposed modification would render *Shin et al.* unsatisfactory for its intended purpose. If *Shin et al.* were assembled in this manner then lead 2 would include a relatively thin wire-bonding protruded zone at an intermediate portion between the side surface of plastic encapsulating part 40 and lead end 4. The wire-bonding protruded zone would be thin, fragile and susceptible to mechanical damage when lead 2 was handled, bent and encapsulated. Moreover, the wire-bonding protruded zone would serve no purpose since the site where bond wire 30 contacts lead 2 is buried within plastic encapsulating part 40, and thus, not exposed.

The Examiner attempts to cure this fundamental deficiency by asserting that *Huang et al.* supplies the necessary motivation by increasing the encapsulating area of the molding compound on the surface of the lead. However, *Huang et al.* forms wire-bonding protruded zone 226 in a portion of lead 202 that would otherwise be exposed, whereas *Shin et al.* provides the site where bond wire 30 contacts lead 2 within plastic encapsulating part 40. Thus, the encapsulating area problem in *Huang et al.* does not exist in *Shin et al.*, and the motivation set forth by the Examiner does not exist.

The proposed modification fails to meet the claim limitations. Claim 41 also recites "a lead that protrudes laterally from and extends through the side surface." Claim 101 recites similar limitations. *Shin et al.* fails to teach or suggest this approach in Figs. 10B or 14, as mentioned above for claim 1.

Therefore, the proposed modification is clearly erroneous.

Claims 47 and 106 (Group II)

Claim 47 distinguishes over *Shin et al.* in view of *Huang et al.* for the reasons set forth above for the Group I claims and further distinguishes over *Shin et al.* in view of *Huang et al.* on its own merits since it recites another limitation that is not disclosed by *Shin et al.* in view of *Huang et al.*

Claim 47 recites "the lead is outside the periphery of the chip." Claim 106 recites similar limitations. *Shin et al.* fails to teach or suggest this approach, as mentioned above for claim 7.

Claims 50 and 110 (Group III)

Claim 50 distinguishes over *Shin et al.* in view of *Huang et al.* for the reasons set forth above for the Group I claims and further distinguishes over *Shin et al.* in view of *Huang et al.* on its own merits since it recites another limitation that is not disclosed by *Shin et al.* in view of *Huang et al.*

Claim 50 recites "the device is devoid of wire bonds, TAB leads and solder joints." Claim 110 recites similar limitations. *Shin et al.* fails to teach or suggest this approach, as mentioned above for claim 10.

Claim 107 (Group IV)

Claim 107 distinguishes over *Shin et al.* in view of *Huang et al.* for the reasons set forth above for the Group I claims and further distinguishes over *Shin et al.* in view of *Huang et al.* on its own merits since it recites another limitation that is not disclosed by *Shin et al.* in view of *Huang et al.*

Claim 107 recites "the terminal is integral with a planar routing line that overlaps the lead and the pad and contacts the lead inside the insulative housing, outside a periphery of the terminal and outside a periphery of the chip." *Shin et al.* fails to teach or suggest a planar routing line that is integral with lead end 4, overlaps the chip pad, overlaps lead 2, and contacts lead 2 inside plastic encapsulating part 40 and outside the periphery of chip 20. Instead, lead 2 is a

single continuous copper trace that is integral with lead end 4, overlaps the chip pad and extends to the side surface of plastic encapsulating part 40. In sustaining this rejection, the Examiner asserts that "Shin et al., as modified, discloses the terminal being integral with a planar routing line that overlaps the lead and the pad and contacts the lead inside the insulative housing, outside a periphery of the terminal and outside a periphery of the chip." This is clearly erroneous.

Claims 51, 59, 111 and 119 (Group V)

Claim 51 distinguishes over *Shin et al.* in view of *Huang et al.* for the reasons set forth above for the Group I claims and further distinguishes over *Shin et al.* in view of *Huang et al.* on its own merits since it recites another limitation that is not disclosed by *Shin et al.* in view of *Huang et al.*

Claim 51 recites "the chip includes an upper surface . . . the upper surface includes a conductive pad . . . the upper surface faces towards the bottom surface . . . [and] a terminal that protrudes downwardly from and extends through the bottom surface." Claim 111 recites similar limitations. *Shin et al.* fails to teach or suggest this approach in Fig. 14, in the event Fig. 14 is relied upon to sustain this rejection.

Claims 57 and 117 (Group VI)

Claim 57 distinguishes over *Shin et al.* in view of *Huang et al.* for the reasons set forth above for the Group V claims and further distinguishes over *Shin et al.* in view of *Huang et al.* on its own merits since it recites another limitation that is not disclosed by *Shin et al.* in view of *Huang et al.*

Claim 57 recites "the lead is outside the periphery of the chip." Claim 117 recites similar limitations. *Shin et al.* fails to teach or suggest this approach, as mentioned above for claim 7.

Claim 58 (Group VII)

Claim 58 distinguishes over *Shin et al.* in view of *Huang et al.* for the reasons set forth above for the Group V claims and further distinguishes over *Shin et al.* in view of *Huang et al.* on its own merits since it recites another limitation that is not disclosed by *Shin et al.* in view of *Huang et al.*

Claim 58 recites "the terminal is integral with a routing line that is plated on the lead inside the insulative housing, outside a periphery of the terminal and outside a periphery of the chip." *Shin et al.* fails to teach or suggest this approach, as mentioned above for claim 18.

Claims 60 and 120 (Group VIII)

Claim 60 distinguishes over *Shin et al.* in view of *Huang et al.* for the reasons set forth above for the Group V claims and further distinguishes over *Shin et al.* in view of *Huang et al.* on its own merits since it recites another limitation that is not disclosed by *Shin et al.* in view of *Huang et al.*

Claim 60 recites "the device is devoid of wire bonds, TAB leads and solder joints." Claim 120 recites similar limitations. *Shin et al.* fails to teach or suggest this approach, as mentioned above for claim 10.

Claim 118 (Group IX)

Claim 118 distinguishes over *Shin et al.* in view of *Huang et al.* for the reasons set forth above for the Group V claims and further distinguishes over *Shin et al.* in view of *Huang et al.* on its own merits since it recites another limitation that is not disclosed by *Shin et al.* in view of *Huang et al.*

Claim 118 recites "the terminal is integral with a planar routing line that overlaps the lead and the pad and contacts the lead inside the insulative housing, outside a periphery of the terminal and outside a periphery of the chip." *Shin et al.* fails to teach or suggest this approach, as mentioned above for claim 107.

4. Section 103 Rejections – Claims 42-44, 52-56, 102-104 and 112-116

Claims 42-44, 52-56, 102-104 and 112-116 are rejected under 35 U.S.C. § 103(a) as being unpatentable over *Shin et al.* in view of *Huang et al.* and *Nakamura et al.*

Claims 42-44 and 102-104 (Group I)

Claims 42-44 and 102-104 distinguish over *Shin et al.* in view of *Huang et al.* and *Nakamura et al.* for the reasons set forth above for claims 1 and 41.

Claims 52-56 and 112-116 (Group II)

Claims 52-56 and 112-116 distinguish over *Shin et al.* in view of *Huang et al.* and *Nakamura et al.* for the reasons set forth above for the Group I claims and further distinguish over *Shin et al.* in view of *Huang et al.* and *Nakamura et al.* on their own merits for the reasons set forth above for claim 51.

5. Section 103 Rejections – Claims 61, 65, 66, 68-71 and 78-80

Claims 61, 65, 66, 68-71 and 78-80 are rejected under 35 U.S.C. § 103(a) as being unpatentable over *Osawa* (Japanese Patent Publication No. 06-097352) in view of *McShane et al.* (U.S. Patent No. 5,157,480).

Osawa

Osawa discloses a plastic molded-type semiconductor device that includes chip 1, bump 3, inner lead 4, middle material 5, outer lead 6 and closure resin 7. Chip 1 includes electrode 2. Inner lead 4 is shaped as a "bird clapper" to absorb heat stress. Inner lead 4 includes an upper heel that is horizontal, overlaps outer lead 6 and is exposed, a lower heel that is horizontal and overlaps chip 1, and a slanted part between the upper and lower heels.

Electrode 2 is connected to inner lead 4 through bump 3, and inner lead 4 is connected to outer lead 6 through middle material 5. Thus, electrode 2 and inner lead 4 are spaced and separated from one another, and inner lead 4 and outer lead 6 are spaced and separated from one another.

Inner lead 4 extends to and is exposed at the upper surface of closure resin 7. Furthermore, inner lead 4 is aligned with the upper surface of closure resin 7. *Osawa* (as translated) states as follows:

> [A]nd it is made to expose the outer edge of an inner lead 4 so that the upper surface may accomplish the same flat surface as the upper surface of the closure resin 7. (Translation, page 2, paragraph 0010, lines 4-7.)

Likewise, inner lead 4 is shown as aligned with the upper surface of closure resin 7 in Fig. 1(B). Thus, inner lead 4 is aligned with but does not protrude from the upper surface of closure resin 7.

McShane et al.

McShane et al. discloses a semiconductor device with dual electrical contact sites.

Semiconductor device 10 includes die 12, lead 14, die receiving area 15, wire bond 16, package body 17 and solder ball 26 in Fig. 1. Lead 14 includes first contact portion 18, second contact portion 20 and intermediate portion 22. First contact portion 18 is substantially flush with the bottom surface, and solder ball 26 protrudes from the bottom surface.

Semiconductor device 30 includes die 32, die receiving area 34, lead 36, wire bond 38 and package body 39. Lead 36 includes first contact portion 42, second contact portion 44 and intermediate portion 46. First contact portion 42 is substantially flush with the bottom surface, and second contact portion 44 can extend upwardly as shown by dashed second contact portion 48.

Claims 71 and 78-80 (Group I)

Claim 71 recites "an insulative housing with a top surface, a bottom surface, and a peripheral side surface between the top and bottom surfaces" and "a terminal that . . . protrudes downwardly from and extends through the bottom surface" and "a lead that protrudes downwardly from and contacts and is not integral with the routing line."

Osawa fails to teach or suggest this approach. Inner lead 4 does not protrude from closure resin 7. Instead, inner lead 4 is aligned with closure resin 7. Furthermore, inner lead 4 does not contact outer lead 6. Instead, inner lead 4 is connected to outer lead 6 through middle material 5. *McShane et al.* fails to cure this deficiency. There is no teaching, suggestion or motivation to modify *Osawa* using the assembly technique taught by *McShane et al.*, and even if there was, the proposed modification would not meet the claim limitations.

In sustaining this rejection, the Examiner states as follows:

> Regarding claim 71, Osawa discloses in Fig. 1 a semiconductor package device, comprising:
> - an insulative housing (7) with a top surface, a bottom surface, and a peripheral side surface between the top and bottom surfaces;
> - a semiconductor chip (1) within and surrounded by the insulative housing, wherein the chip includes an upper surface and a lower surface, the upper surface includes a conductive pad (2), the upper surface faces towards the bottom surface and faces away from the top surface, and the insulative housing contacts the lower surface;
> - a routing line (4) within and surrounded by the insulative housing, wherein the routing line overlaps and is electrically connected to the pad;
> - a terminal (an area of 4 which connected to an element 5) that protrudes downwardly from and is integral with the routing line, protrudes downwardly from and extends through the bottom surface, is spaced from the side surface and is electrically connected to the pad; and
> - a lead (6) that contacts and is not integral with the routing line, protrudes laterally from and extends through the side surface and is electrically connected to the pad, wherein the terminal and the lead are spaced and separated from one another outside the insulative housing, and the terminal and the lead are electrically connected to one another inside the insulative housing and outside the chip.
>
> Osawa does not disclose the lead that protrudes downward. However, McShane et al. discloses in Fig. 2 a lead (48) that protrudes downward. Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Osawa by using the lead to protrude downward as taught by

> McShane et al. The ordinary artisan would have been motivated to modify Osawa in the manner described above for at least the purpose of providing a flexibility in substrate mounting (column 4, lines 50 ~ 51).

The rejection is flawed for several reasons.

The proposed modification is vague and confusing. The proposed modification, as best Applicant can tell, is to bend outer lead 6 in *Osawa et al.* like dashed second contact portion 48 in *McShane et al.* However, outer lead 6 in *Osawa et al.* vertically extends away from inner lead 4 just as dashed second contact portion 48 vertically extends away from first contact portion 42. Therefore, it is unclear what the proposed modification is. Applicant should be given a reasonable explanation of what the proposed modification is rather than be forced to second-guess what it is. For this reason alone, the rejection is improper and should be overturned.

The proposed modification fails to meet the claim limitations.

Claim 71 recites "a terminal that . . . protrudes downwardly from . . . the bottom surface." *Osawa* fails to teach or suggest that inner lead 4 protrudes from closure resin 7. In sustaining this rejection, the Examiner asserts that "a terminal (an area of 4 which is connected to an element 5) . . . protrudes downwardly from . . . the bottom surface." This is clearly erroneous.[2]

Claim 71 also recites "a lead that . . . contacts . . . the routing line." *Osawa* fails to teach or suggest that outer lead 6 contacts inner lead 4. In sustaining this rejection, the Examiner asserts that "a lead (6) that contacts . . . the routing line [4]." This is clearly erroneous.

Claim 71 also recites "a lead that protrudes downwardly from . . . the routing line." As the Examiner admits, *Osawa* fails to teach or suggest that outer lead 6 protrudes "downwardly" (meaning *Osawa* fails to teach or suggest that outer lead 6 protrudes towards the upper surface of

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[2] The Examiner asserts that "Osawa discloses in Fig. 1 . . . an insulative housing (7) with . . . a bottom surface . . . a semiconductor chip (1) . . . [that] includes an upper surface . . . the upper surface includes a conductive pad (2), the upper surface faces towards the bottom surface." Electrode 2 faces towards the upper surface of closure resin 7. Thus, the Examiner characterizes the upper surface of closure resin 7 as the claimed bottom surface. As a result, inner lead 4 would need to protrude upwardly from the upper surface of closure resin 7 in order to meet the claim limitation that the terminal protrudes downwardly from the bottom surface. Inner lead 4 does not protrude upwardly from the upper surface of closure resin 7, and therefore fails to meet the claim limitation.

closure resin 7 where inner lead 4 is exposed). In sustaining this rejection, the Examiner asserts that "McShane et al. discloses in Fig. 2 a lead (48) that protrudes downward." This is clearly erroneous. Dashed second contact portion 48 protrudes away from first contact portion 42.

Moreover, *McShane et al.* fails to teach or suggest that both the bottom-side contact and the peripheral contact protrude below the bottom surface of the package body. In semiconductor device 10, the bottom-side contact (solder ball 26) protrudes below the bottom surface of package body 17 but the peripheral contact (second contact portion 20) does not. In semiconductor device 30, the peripheral contact (second contact portion 44) protrudes below the bottom surface of package body 39 but the bottom-side contact (first contact portion 42) does not. Therefore, even if inner lead 4 protruded from the upper surface of closure resin 7 (although it does not), *McShane et al.* would fail to teach or suggest that both inner lead 4 and outer lead 6 protrude above the upper surface of closure resin 7, or that outer lead 6 protrudes above inner lead 4.

Therefore, the proposed modification is clearly erroneous.

Claims 61, 65, 66 and 68-70 (Group II)

Claim 61 distinguishes over *Osawa* in view of *McShane et al.* for the reasons set forth above for the Group I claims and further distinguishes over *Osawa* in view of *McShane et al.* on its own merits since it recites another limitation that is not disclosed by *Osawa* in view of *McShane et al.*

Claim 61 recites "the terminal and the lead are electrically connected together by the routing line." *Osawa* fails to teach or suggest that the upper heel of inner lead 4 is electrically connected to outer lead 6 by another portion of inner lead 4. Instead, the upper heel of inner lead 4 is electrically connected to outer lead 6 by middle material 5. In sustaining this rejection, the Examiner asserts that "the terminal [an area of 4 which connected to an element 5] and the lead [6] are electrically connected to one another by the routing line [4]." This is clearly erroneous.

6. Section 103 Rejections – Claims 62-64

Claims 62-64 are rejected under 35 U.S.C. § 103(a) as being unpatentable over *Osawa* in view of *McShane et al.* and *Happ* (U.S. Patent No. 3,627,901).

Happ

Happ discloses a combined electronic package device and connector.

Connector member 10 includes indexing apertures 12 and 14, central portion 16 and outer longitudinal edges 18 and 20 in Fig. 1. Coating 21 is used for the embodiment in Fig. 2 but not for the embodiment in Fig. 3.

Connector member 10 is manufactured to include comblike structure 70, partial lead frame structure 80, and web members 90 and 92 in Fig. 3. Comblike structure 70 includes male connector pins 72, 74, 76 and 78. Partial lead frame structure 80 includes lead members 82, 84, 86 and 88. Lead members 82, 84, 86 and 88 include terminal members 94, 96, 98 and 100. Space 102 is located at a common center between the terminal members.

Connector pins 72, 74, 76 and 78 are bent to extend perpendicularly to lead members 82, 84, 86 and 88 and encapsulation material 112 is provided in Fig. 5. Encapsulation material 112 includes cavity 113 that exposes terminal members 94, 96, 98 and 100. Encapsulation material 112 also includes floor 114 that supports lead members 82, 84, 86 and 88.

Semiconductor device 138 is mounted face down and placed in direct electrical contact with and bonded to terminal members 94, 96, 98 and 100 in Fig. 7. Semiconductor device 138 includes various circuit elements that terminate at its face (upper surface) and make direct electrical contact with terminal members 94, 96, 98 and 100, and semiconductor device 138 includes a rear (lower) surface that faces away from terminal members 94, 96, 98 and 100 and is exposed.

Sealant plug 142 seals cavity 113 in Fig. 8. Encapsulation material 140 designates encapsulation material 112. Thus, encapsulation material 140 is spaced and separated from the lower surface of semiconductor device 138, and sealant plug 142 contacts and covers the lower surface of semiconductor device 138. Furthermore, encapsulation material 140 and sealant plug 142 are aligned with one another at the top surface of the structure.

Claims 62 and 64 (Group I)

Claim 62 distinguishes over *Osawa* in view of *McShane et al.* and *Happ* for the reasons set forth above for claim 61 and further distinguishes over *Osawa* in view of *McShane et al.* and *Happ* on its own merits since it recites another limitation that is not disclosed by *Osawa* in view of *McShane et al.* and *Happ.*

Claim 62 recites "the insulative housing includes a first single-piece housing portion that contacts the routing line and the lead and is spaced from the terminal and a second single-piece housing portion that contacts the first single-piece housing portion, the routing line and the terminal."

Osawa fails to teach or suggest this approach. Closure resin 7 does not include a first single-piece housing portion that contacts the slanted part/lower heel of inner lead 4 and outer lead 6 and is spaced from the upper heel of inner lead 4 and a second single-piece housing portion that contacts the first single-piece housing portion and the slanted part/lower heel and the upper heel of inner lead 4. Instead, closure resin 7 is a single-piece that contacts the upper heel, lower heel and slanted part of inner lead 4 and outer lead 6. *McShane et al.* fails to cure this deficiency since package body 39 is a single-piece. *Happ* fails to cure this deficiency since the proposed modification would not meet the claim limitations.

In sustaining this rejection, the Examiner states as follows:

> Regarding claim 62, Osawa, as modified, discloses the claimed invention except for the insulative housing including a first single-piece housing portion that contacts the routing line and the lead and being spaced from the terminal and a second single-piece housing portion that contacts the first single-piece housing portion, the routing line and the terminal. However, Happ discloses in Fig. 7, Fig. 8 and column 9, lines 16 ~ 39 an insulative housing (140 and 142) including a first single-piece housing portion (140) that contacts a routing line (86) and a lead (82) and being spaced from a terminal (100) and a second single-piece housing portion (142) that contacts the first single-piece housing portion, the routing line and the terminal. Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to further modify Osawa by using the first and second single-piece housing portion for the insulative housing as taught by Happ. The ordinary artisan would have been motivated to further modify Osawa in the manner described above for at least the purpose of adding further mechanical strength and rigidity to the overall structure (column 9, lines 24 ~ 25).

The rejection is flawed for several reasons.

The proposed modification, as best Applicant can tell, is to use encapsulation material 140 and sealant plug 142 in *Happ* as closure resin 7 in *Osawa et al.* The proposed modification would require (1) forming encapsulation material 140 that contacts inner lead 4, middle material 5 and outer lead 6 and contains cavity 113 that exposes the lower heel of inner lead 4, (2) disposing chip 1 in cavity 113 such that bump 3 contacts and electrically connects electrode 2 and the lower heel of inner lead 4, and then (3) sealing cavity 113 with sealant plug 142.

As a result, encapsulation material 140 would be spaced from the lower surface of chip 1, encapsulation material 140 would contact the upper heel of inner lead 4, encapsulation material 140 would provide the insulative housing surface where the upper heel of inner lead 4 is exposed, sealant plug 142 would contact and cover the lower surface of chip 1, sealant plug 142 would be spaced from the upper heel of inner lead 4, sealant plug 142 would be spaced from the insulative housing surface where the upper heel of inner lead 4 is exposed, and encapsulation material 140 and sealant plug 142 would be aligned with one another at a flat insulative housing surface.

The proposed modification fails to meet the claim limitations.

Claim 62 recites "a first single-piece housing portion that . . . is spaced from the terminal." *Osawa* fails to teach or suggest this approach if encapsulation material 140 and sealant plug 142 are used as closure resin 7. Instead, encapsulation material 140 would contact the upper heel of inner lead 4. In sustaining this rejection, the Examiner asserts that "a first single-piece housing portion (140) . . . being spaced from a terminal (100)." This is clearly erroneous under the proposed modification. The Examiner has proposed "to further modify Osawa by using the first and second single-piece housing portion of the insulative housing as taught by Happ." The Examiner has not proposed modifying *Osawa* by using the conductors in *Happ*. Therefore, comparing the claimed terminal with terminal member 100 in *Happ* is improper.

Claim 62 also recites "a second single-piece housing portion that contacts . . . the terminal." *Osawa* fails to teach or suggest this approach if encapsulation material 140 and sealant plug 142 are used as closure resin 7. Instead, sealant plug 142 would be spaced from the upper heel of inner lead 4. In sustaining this rejection, the Examiner asserts that "a second single-piece housing portion (142) that contacts . . . the terminal [100]." This is clearly erroneous under the proposed modification. The Examiner has proposed "to further modify Osawa by using the first and second single-piece housing portion of the insulative housing as taught by Happ." The Examiner has not proposed modifying *Osawa* by using the conductors in *Happ*. Therefore, comparing the claimed terminal with terminal member 100 in *Happ* is improper.

Therefore, the proposed modification is clearly erroneous.

Claim 63 (Group II)

Claim 63 distinguishes over *Osawa* in view of *McShane et al.* and *Happ* for the reasons set forth above for the Group I claims and further distinguishes over *Osawa* in view of *McShane et al.* and *Happ* on its own merits since it recites another limitation that is not disclosed by *Osawa* in view of *McShane et al.* and *Happ*.

Claim 63 recites "the first single-piece housing portion contacts the lower surface." *Osawa* fails to teach or suggest this approach if encapsulation material 140 and sealant plug 142 are used as closure resin 7. Instead, encapsulation material 140 would be spaced from the lower (inactive) surface of chip 1. In sustaining this rejection, the Examiner asserts that "Happ discloses in Fig. 7, Fig. 8 and column 9, lines 32 ~ 39 the first single-piece housing portion contacting the lower surface." This is clearly erroneous under the proposed modification and ignores the claim limitations. The Examiner has proposed "to further modify Osawa by using the first and second single-piece housing portion of the insulative housing as taught by Happ." The Examiner has not proposed modifying *Osawa* by using the semiconductor device in *Happ*. Therefore, comparing the claimed lower surface with semiconductor device 138 in *Happ* is improper. Moreover, claim 63 depends from claim 61, which recites "the chip includes an upper surface and a lower surface, and the upper surface includes a conductive pad." Thus, encapsulation material 140 does not contact the lower (inactive) surface of semiconductor device 138 in *Happ*, and under the proposed modification, encapsulation material 140 would not contact the lower (inactive) surface of chip 1 in *Osawa*.

7. Section 103 Rejections – Claims 72-76

Claims 72-76 are rejected under 35 U.S.C. § 103(a) as being unpatentable over *Osawa* in view of *McShane et al.* and *Happ*.

Claims 72, 75 and 76 (Group I)

Claim 72 distinguishes over *Osawa* in view of *McShane et al.* and *Happ* for the reasons set forth above for claim 71 and further distinguishes over *Osawa* in view of *McShane et al.* and *Happ* on its own merits since it recites another limitation that is not disclosed by *Osawa* in view of *McShane et al.* and *Happ*.

Claim 72 recites "the insulative housing consists of a first single-piece housing portion that contacts the lower surface, the routing line and the lead and is spaced from the terminal and a second single-piece housing portion that contacts the first single-piece housing portion, the routing line and the terminal."

Osawa fails to teach or suggest this approach, and *Happ* fails to cure this deficiency, as mentioned above for claims 62 and 63.

Claims 73 and 74 (Group II)

Claim 73 distinguishes over *Osawa* in view of *McShane et al.* and *Happ* for the reasons set forth above for the Group I claims and further distinguishes over *Osawa* in view of *McShane et al.* and *Happ* on its own merits since it recites another limitation that is not disclosed by *Osawa* in view of *McShane et al.* and *Happ*.

Claim 73 recites "the first single-piece housing portion provides the top surface, the side surface and a peripheral portion of the bottom surface, and the second single-piece housing portion provides a central portion of the bottom surface within the peripheral portion of the bottom surface." *Osawa* fails to teach or suggest this approach if encapsulation material 140 and sealant plug 142 are used as closure resin 7. Instead, encapsulation material 140 would provide the bottom surface, the side surface and a peripheral portion of the top surface, and sealant plug 142 would provide a central portion of the top surface within the peripheral portion of the top surface. In sustaining this rejection, the Examiner asserts that "Happ discloses in Fig. 7, Fig. 8 and column 9, lines 32 ~ 39 the first single-piece housing portion providing the top surface, the side surface and a peripheral portion of the bottom surface, and the second single-piece housing portion providing a central portion of the bottom surface within the peripheral portion of the bottom surface." This is clearly erroneous under the proposed modification. The Examiner has proposed "to further modify Osawa by using the first and second single-piece housing portion of the insulative housing as taught by Happ." Moreover, claim 73 depends from claim 71, which recites "a terminal that . . . protrudes downwardly from and extends through the bottom surface." Thus, under the proposed modification, sealant plug 142 would not provide a central portion of the bottom surface. Instead, sealant plug 142 would provide a central portion of the top surface.

8. Section 103 Rejections – Claims 81-87, 89-97, 99 and 100

Claims 81-87, 89-97, 99 and 100 are rejected under 35 U.S.C. § 103(a) as being unpatentable over *Osawa* in view of *McShane et al.* and *Happ.*

Claims 81, 87, 89 and 90 (Group I)

Claim 81 recites "a terminal that . . . protrudes downwardly from . . . the bottom surface." *Osawa* fails to teach or suggest this approach, as mentioned above for claim 71.

Claim 81 also recites "a lead that . . . contacts . . . the routing line." *Osawa* fails to teach or suggest this approach, as mentioned above for claim 71.

Claim 81 also recites "a lead that protrudes downwardly from . . . the routing line." *Osawa* fails to teach or suggest this approach, and *McShane et al.* fails to cure this deficiency, as mentioned above for claim 71.

Claim 81 also recites "the terminal and the lead are electrically connected together by the routing line." *Osawa* fails to teach or suggest this approach, as mentioned above for claim 61.

Claim 81 also recites "an insulative housing with a top surface, a bottom surface, and peripheral side surfaces between the top and bottom surfaces, wherein the bottom surface includes a peripheral portion adjacent to the side surfaces and a central portion within the peripheral portion and spaced from the side surfaces." *Osawa* fails to teach or suggest this approach, and *Happ* fails to cure this deficiency, as mentioned above for claim 73.

Claim 81 also recites "the peripheral portion protrudes downwardly from the central portion." *Osawa* fails to teach or suggest this approach. Closure resin 7 does not include a peripheral portion that protrudes downwardly from a central portion. Instead, closure resin 7 is flat at the top and bottom surfaces. *McShane et al.* fails to cure this deficiency since package body 39 flat at the top and bottom surfaces. *Happ* fails to cure this deficiency since encapsulation material 140 and sealant plug 142 are aligned with one another.

In sustaining this rejection, the Examiner states as follows:

> Regarding claim 81, Osawa discloses in Fig. 1 a semiconductor package device, comprising:
> - an insulative housing (7) with a top surface, a bottom surface, and a peripheral side surface between the top and bottom surfaces;
> - a semiconductor chip (1) within and surrounded by the insulative housing, wherein the chip includes an upper surface and a lower surface, and the upper surface includes a conductive pad (2);
> - a routing line (4) within and surrounded by the insulative housing, wherein the routing line overlaps and is electrically connected to the pad;
> - a terminal (an area of 4 which connected to an element 5) that protrudes downwardly from and is integral with the routing line, protrudes downwardly from and extends through the central portion of the bottom surface, is spaced from the side surface and is electrically connected to the pad; and
> - a lead (6) that contacts and is not integral with the routing line, protrudes laterally from and extends through one of the side surfaces and is electrically connected to the pad, wherein the terminal and the lead are spaced and separated from one another outside the insulative housing, and the terminal and the lead are electrically connected to one another inside the insulative housing and outside the chip.
>
> Osawa does not disclose the lead that protrudes downward. However, McShane et al. discloses in Fig. 2 a lead (48) that protrudes downward. Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Osawa by using the lead to protrude downward as taught by McShane et al. The ordinary artisan would have been motivated to modify Osawa in the manner described above for at least the purpose of providing a flexibility in substrate mounting (column 4, lines 50 ~ 51).
>
> Further, Osawa does not disclose the bottom surface including a peripheral portion adjacent to the side surfaces and a central portion within the peripheral portion and spaced from the side surfaces, and the peripheral portion protrudes downwardly from the central portion. However, Happ discloses in Fig. 5 a bottom

> surface of an insulative housing (112) including a peripheral portion (at the side wall of 113) adjacent to side surfaces and a central portion (113) within the peripheral portion and spaced from the side surfaces, and the peripheral portion protrudes downwardly from the central portion. Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to further modify Osawa by using the peripheral portion to protrude downwardly from the central portion as taught by Happ. The ordinary artisan would have been motivated to further modify Osawa in the manner described above for at least the purpose of enhancing the heat dissipation properties of the unit (column 7, lines 73 ~ 75).

The rejection is flawed for several reasons.

The proposed modification is vague and confusing. The proposed modification, as best Applicant can tell, is to use encapsulation material 140 in *Happ* as closure resin 7 in *Osawa et al.* However, cavity 113 is not a central portion of encapsulation material 140. Therefore, it is unclear what the central portion is. Applicant should be given a reasonable explanation of what the proposed modification is rather than be forced to second-guess what it is. For this reason alone, the rejection is improper and should be overturned.

The proposed modification would require forming encapsulation material 140 that contacts inner lead 4, middle material 5 and outer lead 6 and contains cavity 113 that exposes the lower heel of inner lead 4 to allow disposing chip 1 in cavity 113 such that bump 3 contacts and electrically connects electrode 2 and the lower heel of inner lead 4.

As a result, encapsulation material 140 would be spaced from the lower surface of chip 1, encapsulation material 140 would contact the upper heel of inner lead 4, encapsulation material 140 would provide the insulative housing surface where the upper heel of inner lead 4 is exposed, cavity 113 would expose the lower surface of chip 1, cavity 113 would be spaced from the upper heel of inner lead 4, and cavity 113 would be spaced from the insulative housing surface where the upper heel of inner lead 4 is exposed.

The proposed modification fails to meet the claim limitations.

Claim 81 recites "a semiconductor chip within and surrounded by the insulative housing." In sustaining this rejection, the Examiner asserts that "a semiconductor chip (1) within and surrounded by the insulative housing [7]." This is clearly erroneous under the proposed modification. The Examiner has proposed "to further modify Osawa by using the peripheral portion to protrude downwardly from the central portion as taught by Happ [in Fig. 5]." Under the proposed modification, chip 1 would not be surrounded by encapsulation material 140. Instead, the lower (inactive) surface of chip 1 would be exposed by cavity 113 in encapsulation material 140.

Claim 81 also recites "the peripheral portion protrudes downwardly from the central portion." *Osawa* fails to teach or suggest this approach if encapsulation material 140 is used as closure resin 7. Instead, encapsulation material 140 would provide the bottom surface, the side surface and a peripheral portion of the top surface, and cavity 113 would be exposed at the top surface rather than the bottom surface, as mentioned above for claim 73. Moreover, even if cavity 113 was exposed at the bottom surface (although *Happ* fails to teach this approach), the upper heel of inner lead 4 would not extend into or through cavity 113.

Claims 82 and 85 (Group II)

Claim 82 distinguishes over *Osawa* in view of *McShane et al.* and *Happ* for the reasons set forth above for the Group I claims and further distinguishes over *Osawa* in view of *McShane et al.* and *Happ* on its own merits since it recites another limitation that is not disclosed by *Osawa* in view of *McShane et al.* and *Happ*.

Claim 82 recites "the insulative housing consists of a first single-piece housing portion that contacts the lower surface, the routing line and the lead and is spaced from the terminal and a second single-piece housing portion that contacts the first single-piece housing portion, the routing line and the terminal."

Osawa fails to teach or suggest this approach, and *Happ* fails to cure this deficiency, as mentioned above for claim 72.

Claims 83 and 84 (Group III)

Claim 83 distinguishes over *Osawa* in view of *McShane et al.* and *Happ* for the reasons set forth above for the Group II claims and further distinguishes over *Osawa* in view of *McShane et al.* and *Happ* on its own merits since it recites another limitation that is not disclosed by *Osawa* in view of *McShane et al.* and *Happ*.

Claim 83 recites "the first single-piece housing portion provides the top surface, the side surfaces and the peripheral portion of the bottom surface, and the second single-piece housing portion provides the central portion of the bottom surface."

Osawa fails to teach or suggest this approach, and *Happ* fails to cure this deficiency, as mentioned above for claim 73.

Claims 86, 91, 97, 99 and 100 (Group IV)

Claim 86 distinguishes over *Osawa* in view of *McShane et al.* and *Happ* for the reasons set forth above for the Group I claims and further distinguishes over *Osawa* in view of *McShane et al.* and *Happ* on its own merits since it recites another limitation that is not disclosed by *Osawa* in view of *McShane et al.* and *Happ*.

Claim 86 recites "the peripheral portion of the bottom surface protrudes a first distance below the central portion of the bottom surface, the terminal protrudes a second distance below the central portion of the bottom surface, and the first distance is greater than the second distance." Claim 91 recites similar limitations. The proposed modification fails to teach or suggest that a peripheral portion of the bottom surface protrudes below a central portion of the bottom surface or that the terminal protrudes below a central portion of the bottom surface, as mentioned above for claim 81, much less that a first distance the peripheral portion protrudes is greater than a second distance the terminal protrudes. In sustaining this rejection, the Examiner asserts that "Osawa, as modified, discloses the peripheral portion of the bottom surface protruding a first distance below the central portion of the bottom surface, the terminal protruding a second distance below the central portion of the bottom surface, and the first distance being greater than the second distance." This is clearly erroneous.

Claims 92 and 95 (Group V)

Claim 92 distinguishes over *Osawa* in view of *McShane et al.* and *Happ* for the reasons set forth above for the Group IV claims and further distinguishes over *Osawa* in view of *McShane et al.* and *Happ* on its own merits since it recites another limitation that is not disclosed by *Osawa* in view of *McShane et al.* and *Happ*.

Claim 92 recites "the insulative housing consists of a first single-piece housing portion that contacts the lower surface, the routing line and the lead and is spaced from the terminal and a second single-piece housing portion that contacts the first single-piece housing portion, the routing line and the terminal."

Osawa fails to teach or suggest this approach, and *Happ* fails to cure this deficiency, as mentioned above for claim 72.

Claims 93 and 94 (Group VI)

Claim 93 distinguishes over *Osawa* in view of *McShane et al.* and *Happ* for the reasons set forth above for the Group V claims and further distinguishes over *Osawa* in view of *McShane et al.* and *Happ* on its own merits since it recites another limitation that is not disclosed by *Osawa* in view of *McShane et al.* and *Happ*.

Claim 93 recites "the first single-piece housing portion provides the top surface, the side surfaces and the peripheral portion of the bottom surface, and the second single-piece housing portion provides the central portion of the bottom surface."

Osawa fails to teach or suggest this approach, and *Happ* fails to cure this deficiency, as mentioned above for claim 73.

Claim 96 (Group VII)

Claim 96 distinguishes over *Osawa* in view of *McShane et al.* and *Happ* for the reasons set forth above for the Group IV claims and further distinguishes over *Osawa* in view of

McShane et al. and *Happ* on its own merits since it recites another limitation that is not disclosed by *Osawa* in view of *McShane et al.* and *Happ*.

Claim 96 recites "wherein the first distance is about twice the second distance." *Osawa* fails to teach or suggest this approach, and *Happ* fails to cure this deficiency, as mentioned above for claim 86. In sustaining this rejection, the Examiner asserts that "Osawa, as modified, discloses the first distance being about twice the second distance." This is clearly erroneous.

9. Section 103 Rejections – Claims 67 and 77

Claims 67 and 77 are rejected under 35 U.S.C. § 103(a) as being unpatentable over *Osawa* in view of *McShane et al.* and *Kimura* (U.S. Patent No. 6,218,728).

Kimura

Kimura a ball grid array semiconductor device that includes chip 1, polyimide film 3, laminated metal layer 4, wire 5A, inverted-U-shaped wire 5B, solder ball 6 and resin 7.

Claim 77 (Group I)

Claim 77 distinguishes over *Osawa* in view of *McShane et al.* and *Kimura* for the reasons set forth above for claim 71 and further distinguishes over *Osawa* in view of *McShane et al.* and *Kimura* on its own merits since it recites another limitation that is not disclosed by *Osawa* in view of *McShane et al.* and *Kimura*.

Claim 77 recites "the terminal is within a periphery of the chip."

Osawa fails to teach or suggest this approach. The upper heel of inner lead 4 is outside the periphery of chip 1. *McShane et al.* fails to cure this deficiency since first contact portion 42 is outside the periphery of die 32. *Kimura* fails to cure this deficiency. There is no teaching, suggestion or motivation to modify *Osawa* using the assembly technique taught by *Kimura*, particularly since the proposed modification would render *Osawa* unsatisfactory for its intended purpose.

In sustaining this rejection, the Examiner states as follows:

> Regarding claims 67 and 77, Osawa discloses in Fig. 1 the terminal being outside a periphery of the pad, the routing line being within and outside the periphery of the chip, and the lead being outside the periphery of the chip. Osawa does not disclose the terminal being within a periphery of the chip. However, Kimura discloses in Fig. 4E a terminal (an exposed are of 5B from a resin 7) being within a periphery of a chip (1). Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to further modify Osawa by using the terminal to be within a periphery of the chip as taught by Kimura. The ordinary artisan would have been motivated to further modify Osawa in the manner described above for at least the purpose of increasing speed of I/O signals.

The rejection is flawed for several reasons.

The proposed modification, as best Applicant can tell, is to position the upper heel of inner lead 4 within the periphery of chip 1.

The proposed modification is not taught or suggested by *Kimura*, has no motivation and would render *Osawa* unsatisfactory for its intended purpose, and fails to meet the claim limitations.

Kimura fails to teach or suggest the proposed modification. *Kimura* fails to teach or suggest that inverted-U-shaped wire 5B can be used to connect an outer lead that protrudes from a side surface of resin 7. Instead, inverted-U-shaped wire 5B is used to support solder ball 6 in a ball grid array. Thus, *Kimura* fails to teach or suggest positioning the upper heel of inner lead 4 within the periphery of chip 1.

The proposed modification would render *Osawa* unsatisfactory for its intended purpose. If *Osawa* positioned the upper heel of inner lead 4 within the periphery of chip 1 then inner lead 4 would no longer be shaped as a "bird clapper" to absorb heat stress, thereby rendering *Osawa* unsatisfactory for its intended purpose.

The Examiner attempts to cure this fundamental deficiency by asserting that *Kimura* supplies the necessary motivation by increasing I/O speed of signals. However, bending inner lead 4 to position the upper heel within the periphery of chip 1 would lengthen the signal path to outer lead 6 outside closure resin 7. Moreover, this alternation to inner lead 4 would eliminate the "bird clapper" shape. Thus, the motivation set forth by the Examiner does not exist.

The proposed modification fails to meet the claim limitations. Claim 77 recites "the lead is outside the periphery of the chip." *Osawa* fails to teach or suggest this approach if the upper heel of inner lead 4 is positioned within the periphery of chip 1. Instead, outer lead 6 would extend within the periphery of chip 1. In sustaining this rejection, the Examiner asserts that "Osawa discloses in Fig. 1 . . . the lead being outside the periphery of the chip." This is clearly erroneous under the proposed modification.

Therefore, the proposed modification is clearly erroneous.

Claim 67 (Group II)

Claim 67 distinguishes over *Osawa* in view of *McShane et al.* and *Kimura* for the reasons set forth above for the Group I claim and further distinguishes over *Osawa* in view of *McShane et al.* and *Kimura* on its own merits for the reasons set forth above for claim 61.

10. Section 103 Rejections – Claims 88 and 98

Claims 88 and 98 are rejected under 35 U.S.C. § 103(a) as being unpatentable over *Osawa* in view of *Happ*, *McShane et al.* and *Kimura*.

Claim 88 (Group I)

Claim 88 distinguishes over *Osawa* in view of *Happ*, *McShane et al.* and *Kimura* for the reasons set forth above for claim 81 and further distinguishes over *Osawa* in view of *Happ*, *McShane et al.* and *Kimura* on its own merits since it recites another limitation that is not disclosed by *Osawa* in view of *Happ*, *McShane et al.* and *Kimura*.

Claim 88 recites "the terminal is within a periphery of the chip." *Osawa* fails to teach or suggest this approach, and *Kimura* fails to cure this deficiency, as mentioned above for claim 77.

Claim 98 (Group II)

Claim 98 distinguishes over *Osawa* in view of *Happ*, *McShane et al.* and *Kimura* for the reasons set forth above for the Group I claim and further distinguishes over *Osawa* in view of *Happ, McShane et al.* and *Kimura* on its own merits for the reasons set forth above for claim 86.

Conclusion

To establish prima facie obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine the reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on Applicant's disclosure. See M.P.E.P. § 2142.

It is insufficient that the prior art shows similar components unless it also contains some teaching, suggestion or incentive for arriving at the claimed structure. See *Northern Telecom, Inc. v. Datapoint Corp.*, 908 F.2d 931, 934 (Fed. Cir. 1990).

Moreover, if the proposed modification would render the prior art unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification. See M.P.E.P. § 2143.01.

For the reasons given above, Applicant respectfully submits that claims 1-120 are in condition for allowance and respectfully requests that the outstanding rejections be overturned.

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as First Class Mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on August 29, 2003.

D Sigmond — 8/29/03

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Date of Signature

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IX. APPENDIX OF CLAIMS INVOLVED IN THE APPEAL

1. A semiconductor package device, comprising:

an insulative housing with a top surface, a bottom surface, and a peripheral side surface between the top and bottom surfaces, wherein the insulative housing includes a first single-piece housing portion and a second single-piece housing portion;

a semiconductor chip within the insulative housing, wherein the chip includes an upper surface and a lower surface, and the upper surface includes a conductive pad;

a terminal that protrudes downwardly from and extends through the bottom surface and is electrically connected to the pad; and

a lead that protrudes laterally from and extends through the side surface and is electrically connected to the pad, wherein the first single-piece housing portion contacts the lead and is spaced from the terminal, the second single-piece housing portion contacts the first single-piece housing portion and the terminal, the terminal and the lead are spaced and separated from one another outside the insulative housing, and the terminal and the lead are electrically connected to one another inside the insulative housing and outside the chip.

2. The device of claim 1, wherein the first single-piece housing portion provides the top surface, the side surface and a peripheral portion of the bottom surface, and the second single-piece housing portion provides a central portion of the bottom surface within the peripheral portion of the bottom surface.

3. The device of claim 1, wherein the first single-piece housing portion contacts the lower surface.

4. The device of claim 1, wherein the insulative housing consists of the first and second single-piece housing portions.

5. The device of claim 1, wherein the terminal is the only electrical conductor that extends through the top or bottom surfaces and is electrically connected to the pad.

6. The device of claim 1, wherein the terminal is a plated metal.

7. The device of claim 1, wherein the terminal is within a periphery of the chip, and the lead is outside the periphery of the chip.

8. The device of claim 1, wherein the device is devoid of an electrical conductor that extends through the top surface and is electrically connected to the pad.

9. The device of claim 1, wherein the device includes a plurality of terminals and leads, the chip includes a plurality of pads, each of the terminals are electrically connected to one of the leads and one of the pads inside the insulative housing and outside the chip, the terminals are arranged as an array that protrudes downwardly from and extends through the bottom surface, and the leads are arranged as TSOP leads that protrude laterally from and extend through the side surface and an opposing peripheral side surface of the insulative housing.

10. The device of claim 1, wherein the device is devoid of wire bonds, TAB leads and solder joints.

11. A semiconductor package device, comprising:

an insulative housing with a top surface, a bottom surface, and a peripheral side surface between the top and bottom surfaces, wherein the insulative housing consists of a first single-piece housing portion and a second single-piece housing portion;

a semiconductor chip within and surrounded by the insulative housing, wherein the chip includes an upper surface and a lower surface, the upper surface includes a conductive pad, the upper surface faces towards the bottom surface and faces away from the top surface, and the insulative housing contacts the lower surface;

a terminal that protrudes downwardly from and extends through the bottom surface and is spaced from the side surface and is electrically connected to the pad; and

a lead that protrudes laterally from and extends through the side surface and is electrically connected to the pad, wherein the first single-piece housing portion contacts the lower surface and the lead and is spaced from the terminal, the second single-piece housing portion contacts the first single-piece housing portion and the terminal, the terminal and the lead are spaced and separated from one another outside the insulative housing, and the terminal and the lead are electrically connected to one another inside the insulative housing and outside the chip.

12. The device of claim 11, wherein the first single-piece housing portion is farther from the top surface than the lower surface is from the top surface.

13. The device of claim 11, wherein the first single-piece housing portion provides the top surface, the side surface and a peripheral portion of the bottom surface, and the second single-piece housing portion provides a central portion of the bottom surface within the peripheral portion of the bottom surface.

14. The device of claim 13, wherein the peripheral portion of the bottom surface is outside a periphery of the chip, and the central portion of the bottom surface is within and outside the periphery of the chip.

15. The device of claim 11, wherein the first single-piece housing portion is a transfer molded material, and the second single-piece housing portion is not a transfer molded material.

16. The device of claim 11, wherein the second single-piece housing portion includes first and second opposing surfaces, the first surface contacts the lead and the second surface provides a portion of the bottom surface.

17. The device of claim 11, wherein the terminal is within a periphery of the chip and outside a periphery of the pad, and the lead is outside the periphery of the chip.

18. The device of claim 11, wherein the terminal is integral with a routing line that is plated on the lead inside the insulative housing, outside a periphery of the terminal and outside a periphery of the chip.

19. The device of claim 11, wherein the device includes a plurality of terminals and leads, the chip includes a plurality of pads, each of the terminals are electrically connected to one of the leads and one of the pads inside the insulative housing and outside the chip, the terminals are arranged as an array that protrudes downwardly from and extends through the bottom surface, and the leads are arranged as TSOP leads that protrude laterally from and extend through the side surface and an opposing peripheral side surface of the insulative housing.

20. The device of claim 11, wherein the device is devoid of wire bonds, TAB leads and solder joints.

21. A semiconductor package device, comprising:

an insulative housing with a top surface, a bottom surface, and peripheral side surfaces between the top and bottom surfaces, wherein the bottom surface includes a peripheral portion adjacent to the side surfaces and a central portion within the peripheral portion and spaced from the side surfaces, and the peripheral portion protrudes downwardly from the central portion;

a semiconductor chip within and surrounded by the insulative housing, wherein the chip includes an upper surface and a lower surface, and the upper surface includes a conductive pad;

a terminal that protrudes downwardly from and extends through the central portion of the bottom surface and is spaced from the side surfaces and is electrically connected to the pad; and

a lead that protrudes laterally from and extends through one of the side surfaces and is electrically connected to the pad, wherein the terminal and the lead are spaced and separated from one another outside the insulative housing, and the terminal and the lead are electrically connected to one another inside the insulative housing and outside the chip.

22. The device of claim 21, wherein the insulative housing consists of a first single-piece housing portion that contacts the lower surface and the lead and is spaced from the terminal and a second single-piece housing portion that contacts the first single-piece housing portion and the terminal.

23. The device of claim 22, wherein the first single-piece housing portion provides the top surface, the side surfaces and the peripheral portion of the bottom surface, and the second single-piece housing portion provides the central portion of the bottom surface.

24. The device of claim 23, wherein the peripheral portion of the bottom surface is outside a periphery of the chip, and the central portion of the bottom surface is within and outside the periphery of the chip.

25. The device of claim 22, wherein the first single-piece housing portion is a transfer molded material, and the second single-piece housing portion is not a transfer molded material.

26. The device of claim 21, wherein the peripheral portion of the bottom surface protrudes a first distance below the central portion of the bottom surface, the terminal protrudes a second distance below the central portion of the bottom surface, and the first distance is greater than the second distance.

27. The device of claim 21, wherein the peripheral portion of the bottom surface is shaped as a rectangular peripheral ledge.

28. The device of claim 21, wherein the terminal is within a periphery of the chip, and the peripheral portion of the bottom surface is outside the periphery of the chip.

29. The device of claim 21, wherein the device includes a plurality of terminals and leads, the chip includes a plurality of pads, each of the terminals are electrically connected to one of the leads and one of the pads inside the insulative housing and outside the chip, the terminals

are arranged as an array that protrudes downwardly from and extends through the central portion of the bottom surface, and the leads are arranged as TSOP leads that protrude laterally from and extend through two of the side surfaces that oppose one another.

30. The device of claim 21, wherein the device is devoid of wire bonds, TAB leads and solder joints.

31. A semiconductor package device, comprising:

an insulative housing with a top surface, a bottom surface, and four peripheral side surfaces between the top and bottom surfaces, wherein the bottom surface includes a peripheral portion shaped as a rectangular peripheral ledge adjacent to the side surfaces and a recessed central portion within the peripheral portion and spaced from the side surfaces, and the peripheral portion protrudes downwardly from the central portion and extends a first distance below the central portion;

a semiconductor chip within and surrounded by the insulative housing, wherein the chip includes an upper surface and a lower surface, the upper surface includes a conductive pad, the upper surface faces towards the bottom surface and faces away from the top surface, and the insulative housing contacts the lower surface;

a terminal that protrudes downwardly from and extends through the central portion of the bottom surface and is spaced from the side surfaces and is electrically connected to the pad, wherein the terminal extends a second distance below the central portion, and the first distance is greater than the second distance; and

a lead that protrudes laterally from and extends through one of the side surfaces and is electrically connected to the pad, wherein the terminal and the lead are spaced and separated from one another outside the insulative housing, and the terminal and the lead are electrically connected to one another inside the insulative housing and outside the chip.

32. The device of claim 31, wherein the insulative housing consists of a first single-piece housing portion that contacts the lower surface and the lead and is spaced from the terminal

and a second single-piece housing portion that contacts the first single-piece housing portion and the terminal.

33. The device of claim 32, wherein the first single-piece housing portion provides the top surface, the side surfaces and the peripheral portion of the bottom surface, and the second single-piece housing portion provides the central portion of the bottom surface.

34. The device of claim 33, wherein the peripheral portion of the bottom surface is outside a periphery of the chip, and the central portion of the bottom surface is within and outside the periphery of the chip.

35. The device of claim 32, wherein the first single-piece housing portion is a transfer molded material, and the second single-piece housing portion is not a transfer molded material.

36. The device of claim 31, wherein the first distance is about twice the second distance.

37. The device of claim 31, wherein the peripheral portion of the bottom surface is integral with the side surfaces and non-integral with the central portion of the bottom surface.

38. The device of claim 31, wherein the terminal is within a periphery of the chip, and the peripheral portion of the bottom surface is outside the periphery of the chip.

39. The device of claim 31, wherein the device includes a plurality of terminals and leads, the chip includes a plurality of pads, each of the terminals are electrically connected to one of the leads and one of the pads inside the insulative housing and outside the chip, the terminals are arranged as an array that protrudes downwardly from and extends through the central portion of the bottom surface, and the leads are arranged as TSOP leads that protrude laterally from and extend through two of the side surfaces that oppose one another.

40. The device of claim 31, wherein the device is devoid of wire bonds, TAB leads and solder joints.

41. A semiconductor package device, comprising:

an insulative housing with a top surface, a bottom surface, and a peripheral side surface between the top and bottom surfaces;

a semiconductor chip within the insulative housing, wherein the chip includes an upper surface and a lower surface, and the upper surface includes a conductive pad;

a terminal that protrudes downwardly from and extends through the bottom surface and is electrically connected to the pad; and

a lead that protrudes laterally from and extends through the side surface and is electrically connected to the pad, wherein the lead includes a recessed portion that contacts and extends into the insulative housing and is spaced from the top and bottom surfaces and does not overlap the chip and a non-recessed portion that contacts and extends outside the insulative housing and is adjacent to the recessed portion and the bottom surface, the terminal and the lead are spaced and separated from one another outside the insulative housing, and the terminal and the lead are electrically connected to one another inside the insulative housing and outside the chip.

42. The device of claim 41, wherein the insulative housing includes a first single-piece housing portion that contacts the lead and is spaced from the terminal and a second single-piece housing portion that contacts the first single-piece housing portion and the terminal.

43. The device of claim 42, wherein the first single-piece housing portion contacts the lower surface.

44. The device of claim 42, wherein the insulative housing consists of the first and second single-piece housing portions.

45. The device of claim 41, wherein the terminal is the only electrical conductor that extends through the top or bottom surfaces and is electrically connected to the pad.

46. The device of claim 41, wherein the terminal is a plated metal.

47. The device of claim 41, wherein the terminal is within a periphery of the chip, and the lead is outside the periphery of the chip.

48. The device of claim 41, wherein the device is devoid of an electrical conductor that extends through the top surface and is electrically connected to the pad.

49. The device of claim 41, wherein the device includes a plurality of terminals and leads, the chip includes a plurality of pads, each of the terminals are electrically connected to one of the leads and one of the pads inside the insulative housing and outside the chip, the terminals are arranged as an array that protrudes downwardly from and extends through the bottom surface, and the leads are arranged as TSOP leads that protrude laterally from and extend through the side surface and an opposing peripheral side surface of the insulative housing.

50. The device of claim 41, wherein the device is devoid of wire bonds, TAB leads and solder joints.

51. A semiconductor package device, comprising:

an insulative housing with a top surface, a bottom surface, and a peripheral side surface between the top and bottom surfaces;

a semiconductor chip within and surrounded by the insulative housing, wherein the chip includes an upper surface and a lower surface, the upper surface includes a conductive pad, the upper surface faces towards the bottom surface and faces away from the top surface, and the insulative housing contacts the lower surface;

a terminal that protrudes downwardly from and extends through the bottom surface and is spaced from the side surface and is electrically connected to the pad; and

a lead that protrudes laterally from and extends through the side surface and is electrically connected to the pad, wherein the lead includes a recessed portion that contacts and extends into

the insulative housing and is spaced from the top and bottom surfaces and does not overlap the chip and a non-recessed portion that contacts and extends outside the insulative housing and is adjacent to the recessed portion and the bottom surface, the terminal and the lead are spaced and separated from one another outside the insulative housing, and the terminal and the lead are electrically connected to one another inside the insulative housing and outside the chip.

52. The device of claim 51, wherein the insulative housing consists of a first single-piece housing portion that contacts the lower surface and the lead and is spaced from the terminal and a second single-piece housing portion that contacts the first single-piece housing portion and the terminal.

53. The device of claim 52, wherein the first single-piece housing portion provides the top surface, the side surface and a peripheral portion of the bottom surface, and the second single-piece housing portion provides a central portion of the bottom surface within the peripheral portion of the bottom surface.

54. The device of claim 53, wherein the peripheral portion of the bottom surface is outside a periphery of the chip, and the central portion of the bottom surface is within and outside the periphery of the chip.

55. The device of claim 52, wherein the first single-piece housing portion is a transfer molded material, and the second single-piece housing portion is not a transfer molded material.

56. The device of claim 52, wherein the second single-piece housing portion includes first and second opposing surfaces, the first surface contacts the lead and the second surface provides a portion of the bottom surface.

57. The device of claim 51, wherein the terminal is within a periphery of the chip and outside a periphery of the pad, and the lead is outside the periphery of the chip.

58. The device of claim 51, wherein the terminal is integral with a routing line that is plated on the lead inside the insulative housing, outside a periphery of the terminal and outside a periphery of the chip.

59. The device of claim 51, wherein the device includes a plurality of terminals and leads, the chip includes a plurality of pads, each of the terminals are electrically connected to one of the leads and one of the pads inside the insulative housing and outside the chip, the terminals are arranged as an array that protrudes downwardly from and extends through the bottom surface, and the leads are arranged as TSOP leads that protrude laterally from and extend through the side surface and an opposing peripheral side surface of the insulative housing.

60. The device of claim 51, wherein the device is devoid of wire bonds, TAB leads and solder joints.

61. A semiconductor package device, comprising:

an insulative housing with a top surface, a bottom surface, and a peripheral side surface between the top and bottom surfaces;

a semiconductor chip within the insulative housing, wherein the chip includes an upper surface and a lower surface, and the upper surface includes a conductive pad;

a routing line within the insulative housing that overlaps and is electrically connected to the pad;

a terminal that protrudes downwardly from and is integral with the routing line, protrudes downwardly from and extends through the bottom surface and is electrically connected to the pad; and

a lead that protrudes downwardly from and contacts and is not integral with the routing line, protrudes laterally from and extends through the side surface and is electrically connected to the pad, wherein the terminal and the lead are spaced and separated from one another outside the insulative housing, and the terminal and the lead are electrically connected to one another by the routing line inside the insulative housing and outside the chip.

62. The device of claim 61, wherein the insulative housing includes a first single-piece housing portion that contacts the routing line and the lead and is spaced from the terminal and a second single-piece housing portion that contacts the first single-piece housing portion, the routing line and the terminal.

63. The device of claim 62, wherein the first single-piece housing portion contacts the lower surface.

64. The device of claim 62, wherein the insulative housing consists of the first and second single-piece housing portions.

65. The device of claim 61, wherein the terminal is the only electrical conductor that extends through the top or bottom surfaces and is electrically connected to the pad.

66. The device of claim 61, wherein the routing line and the terminal are a plated metal.

67. The device of claim 61, wherein the terminal is within a periphery of the chip, the routing line is within and outside the periphery of the chip, and the lead is outside the periphery of the chip.

68. The device of claim 61, wherein the device is devoid of an electrical conductor that extends through the top surface and is electrically connected to the pad.

69. The device of claim 61, wherein the device includes a plurality of terminals and leads, the chip includes a plurality of pads, each of the terminals are electrically connected to one of the leads and one of the pads inside the insulative housing and outside the chip, the terminals are arranged as an array that protrudes downwardly from and extends through the bottom surface, and the leads are arranged as TSOP leads that protrude laterally from and extend through the side surface and an opposing peripheral side surface of the insulative housing.

70. The device of claim 61, wherein the device is devoid of wire bonds, TAB leads and solder joints.

71. A semiconductor package device, comprising:

an insulative housing with a top surface, a bottom surface, and a peripheral side surface between the top and bottom surfaces;

a semiconductor chip within and surrounded by the insulative housing, wherein the chip includes an upper surface and a lower surface, the upper surface includes a conductive pad, the upper surface faces towards the bottom surface and faces away from the top surface, and the insulative housing contacts the lower surface;

a routing line within and surrounded by the insulative housing, wherein the routing line overlaps and is electrically connected to the pad;

a terminal that protrudes downwardly from and is integral with the routing line, protrudes downwardly from and extends through the bottom surface, is spaced from the side surface and is electrically connected to the pad; and

a lead that protrudes downwardly from and contacts and is not integral with the routing line, protrudes laterally from and extends through the side surface and is electrically connected to the pad, wherein the terminal and the lead are spaced and separated from one another outside the insulative housing, and the terminal and the lead are electrically connected to one another inside the insulative housing and outside the chip.

72. The device of claim 71, wherein the insulative housing consists of a first single-piece housing portion that contacts the lower surface, the routing line and the lead and is spaced from the terminal and a second single-piece housing portion that contacts the first single-piece housing portion, the routing line and the terminal.

73. The device of claim 72, wherein the first single-piece housing portion provides the top surface, the side surface and a peripheral portion of the bottom surface, and the second

single-piece housing portion provides a central portion of the bottom surface within the peripheral portion of the bottom surface.

74. The device of claim 73, wherein the peripheral portion of the bottom surface is outside a periphery of the chip, and the central portion of the bottom surface is within and outside the periphery of the chip.

75. The device of claim 72, wherein the first single-piece housing portion is a transfer molded material, and the second single-piece housing portion is not a transfer molded material.

76. The device of claim 72, wherein the second single-piece housing portion includes first and second opposing surfaces, the first surface contacts the routing line and the second surface provides a portion of the bottom surface.

77. The device of claim 71, wherein the terminal is within a periphery of the chip and outside a periphery of the pad, the routing line is within and outside the periphery of the chip, and the lead is outside the periphery of the chip.

78. The device of claim 71, wherein the routing line is plated on the lead inside the insulative housing, outside a periphery of the terminal and outside a periphery of the chip.

79. The device of claim 71, wherein the device includes a plurality of terminals and leads, the chip includes a plurality of pads, each of the terminals are electrically connected to one of the leads and one of the pads inside the insulative housing and outside the chip, the terminals are arranged as an array that protrudes downwardly from and extends through the bottom surface, and the leads are arranged as TSOP leads that protrude laterally from and extend through the side surface and an opposing peripheral side surface of the insulative housing.

80. The device of claim 71, wherein the device is devoid of wire bonds, TAB leads and solder joints.

81. A semiconductor package device, comprising:

an insulative housing with a top surface, a bottom surface, and peripheral side surfaces between the top and bottom surfaces, wherein the bottom surface includes a peripheral portion adjacent to the side surfaces and a central portion within the peripheral portion and spaced from the side surfaces, and the peripheral portion protrudes downwardly from the central portion;

a semiconductor chip within and surrounded by the insulative housing, wherein the chip includes an upper surface and a lower surface, and the upper surface includes a conductive pad;

a routing line within and surrounded by the insulative housing, wherein the routing line overlaps and is electrically connected to the pad;

a terminal that protrudes downwardly from and is integral with the routing line, protrudes downwardly from and extends through the central portion of the bottom surface, is spaced from the side surfaces and is electrically connected to the pad; and

a lead that protrudes downwardly from and contacts and is not integral with the routing line, protrudes laterally from and extends through one of the side surfaces and is electrically connected to the pad, wherein the terminal and the lead are spaced and separated from one another outside the insulative housing, and the terminal and the lead are electrically connected to one another by the routing line inside the insulative housing and outside the chip.

82. The device of claim 81, wherein the insulative housing consists of a first single-piece housing portion that contacts the lower surface, the routing line and the lead and is spaced from the terminal and a second single-piece housing portion that contacts the first single-piece housing portion, the routing line and the terminal.

83. The device of claim 82, wherein the first single-piece housing portion provides the top surface, the side surfaces and the peripheral portion of the bottom surface, and the second single-piece housing portion provides the central portion of the bottom surface.

84. The device of claim 83, wherein the peripheral portion of the bottom surface is outside a periphery of the chip, and the central portion of the bottom surface is within and outside the periphery of the chip.

85. The device of claim 82, wherein the first single-piece housing portion is a transfer molded material, and the second single-piece housing portion is not a transfer molded material.

86. The device of claim 81, wherein the peripheral portion of the bottom surface protrudes a first distance below the central portion of the bottom surface, the terminal protrudes a second distance below the central portion of the bottom surface, and the first distance is greater than the second distance.

87. The device of claim 81, wherein the peripheral portion of the bottom surface is shaped as a rectangular peripheral ledge.

88. The device of claim 81, wherein the terminal is within a periphery of the chip, the routing line is within and outside the periphery of the chip, the lead is outside the periphery of the chip, and the peripheral portion of the bottom surface is outside the periphery of the chip.

89. The device of claim 81, wherein the device includes a plurality of terminals and leads, the chip includes a plurality of pads, each of the terminals are electrically connected to one of the leads and one of the pads inside the insulative housing and outside the chip, the terminals are arranged as an array that protrudes downwardly from and extends through the central portion of the bottom surface, and the leads are arranged as TSOP leads that protrude laterally from and extend through two of the side surfaces that oppose one another.

90. The device of claim 81, wherein the device is devoid of wire bonds, TAB leads and solder joints.

91. A semiconductor package device, comprising:

an insulative housing with a top surface, a bottom surface, and four peripheral side surfaces between the top and bottom surfaces, wherein the bottom surface includes a peripheral portion shaped as a rectangular peripheral ledge adjacent to the side surfaces and a recessed central portion within the peripheral portion and spaced from the side surfaces, and the peripheral portion protrudes downwardly from the central portion and extends a first distance below the central portion;

a semiconductor chip within and surrounded by the insulative housing, wherein the chip includes an upper surface and a lower surface, the upper surface includes a conductive pad, the upper surface faces towards the bottom surface and faces away from the top surface, and the insulative housing contacts the lower surface;

a routing line within and surrounded by the insulative housing, wherein the routing line overlaps and is electrically connected to the pad;

a terminal that protrudes downwardly from and is integral with the routing line, protrudes downwardly from and extends through the central portion of the bottom surface, is spaced from the side surfaces and is electrically connected to the pad, wherein the terminal extends a second distance below the central portion, and the first distance is greater than the second distance; and

a lead that protrudes downwardly from and contacts and is not integral with the routing line, protrudes laterally from and extends through one of the side surfaces and is electrically connected to the pad, wherein the terminal and the lead are spaced and separated from one another outside the insulative housing, and the terminal and the lead are electrically connected to one another by the routing line inside the insulative housing and outside the chip.

92. The device of claim 91, wherein the insulative housing consists of a first single-piece housing portion that contacts the lower surface, the routing line and the lead and is spaced from the terminal and a second single-piece housing portion that contacts the first single-piece housing portion, the routing line and the terminal.

93. The device of claim 92, wherein the first single-piece housing portion provides the top surface, the side surfaces and the peripheral portion of the bottom surface, and the second single-piece housing portion provides the central portion of the bottom surface.

94. The device of claim 93, wherein the peripheral portion of the bottom surface is outside a periphery of the chip, and the central portion of the bottom surface is within and outside the periphery of the chip.

95. The device of claim 92, wherein the first single-piece housing portion is a transfer molded material, and the second single-piece housing portion is not a transfer molded material.

96. The device of claim 91, wherein the first distance is about twice the second distance.

97. The device of claim 91, wherein the peripheral portion of the bottom surface is integral with the side surfaces and non-integral with the central portion of the bottom surface.

98. The device of claim 91, wherein the terminal is within a periphery of the chip, the routing line is within and outside the periphery of the chip, the lead is outside the periphery of the chip, and the peripheral portion of the bottom surface is outside the periphery of the chip.

99. The device of claim 91, wherein the device includes a plurality of terminals and leads, the chip includes a plurality of pads, each of the terminals are electrically connected to one of the leads and one of the pads inside the insulative housing and outside the chip, the terminals are arranged as an array that protrudes downwardly from and extends through the central portion of the bottom surface, and the leads are arranged as TSOP leads that protrude laterally from and extend through two of the side surfaces that oppose one another.

100. The device of claim 91, wherein the device is devoid of wire bonds, TAB leads and solder joints.

101. A semiconductor package device, comprising:

an insulative housing with a top surface, a bottom surface, and a peripheral side surface between the top and bottom surfaces;

a semiconductor chip within the insulative housing, wherein the chip includes an upper surface and a lower surface, and the upper surface includes a conductive pad;

a terminal that protrudes downwardly from and extends through the bottom surface and is electrically connected to the pad; and

a lead that protrudes laterally from and extends through the side surface and is electrically connected to the pad, wherein the lead includes a recessed portion that extends into the insulative housing and is spaced from the top and bottom surfaces and a non-recessed portion that extends outside the insulative housing and is adjacent to the recessed portion and contacts the insulative housing, the recessed and non-recessed portions each include four outer surfaces, three of the outer surfaces of the recessed and non-recessed portions that do not face in the same direction as the bottom surface are coplanar with one another where the recessed and non-recessed portions are adjacent to one another, one of the outer surfaces of the recessed and non-recessed portions that face in the same direction as the bottom surface are not coplanar with one another where the recessed and non-recessed portions are adjacent to one another, the terminal and the lead are spaced and separated from one another outside the insulative housing, and the terminal and the lead are electrically connected to one another inside the insulative housing and outside the chip.

102. The device of claim 101, wherein the insulative housing includes a first single-piece housing portion that contacts the lead and is spaced from the terminal and a second single-piece housing portion that contacts the first single-piece housing portion and the terminal.

103. The device of claim 102, wherein the first single-piece housing portion contacts the lower surface.

104. The device of claim 102, wherein the insulative housing consists of the first and second single-piece housing portions.

105. The device of claim 101, wherein the terminal is the only electrical conductor that extends through the top or bottom surfaces and is electrically connected to the pad.

106. The device of claim 101, wherein the terminal is within a periphery of the chip, and the lead is outside the periphery of the chip.

107. The device of claim 101, wherein the terminal is integral with a planar routing line that overlaps the lead and the pad and contacts the lead inside the insulative housing, outside a periphery of the terminal and outside a periphery of the chip.

108. The device of claim 101, wherein the device is devoid of an electrical conductor that extends through the top surface and is electrically connected to the pad.

109. The device of claim 101, wherein the device includes a plurality of terminals and leads, the chip includes a plurality of pads, each of the terminals are electrically connected to one of the leads and one of the pads inside the insulative housing and outside the chip, the terminals are arranged as an array that protrudes downwardly from and extends through the bottom surface, and the leads are arranged as TSOP leads that protrude laterally from and extend through the side surface and an opposing peripheral side surface of the insulative housing.

110. The device of claim 101, wherein the device is devoid of wire bonds, TAB leads and solder joints.

111. A semiconductor package device, comprising:

an insulative housing with a top surface, a bottom surface, and a peripheral side surface between the top and bottom surfaces;

a semiconductor chip within and surrounded by the insulative housing, wherein the chip includes an upper surface and a lower surface, the upper surface includes a conductive pad, the upper surface faces towards the bottom surface and faces away from the top surface, and the insulative housing contacts the lower surface;

a terminal that protrudes downwardly from and extends through the bottom surface and is spaced from the side surface and is electrically connected to the pad; and

a lead that protrudes laterally from and extends through the side surface and is electrically connected to the pad, wherein the lead includes a recessed portion that extends into the insulative housing and is spaced from the top and bottom surfaces and a non-recessed portion that extends outside the insulative housing and is adjacent to the recessed portion and contacts the insulative housing, the recessed and non-recessed portions each include four outer surfaces, three of the outer surfaces of the recessed and non-recessed portions that do not face in the same direction as the bottom surface are coplanar with one another where the recessed and non-recessed portions are adjacent to one another, one of the outer surfaces of the recessed and non-recessed portions that face in the same direction as the bottom surface are not coplanar with one another where the recessed and non-recessed portions are adjacent to one another, the terminal and the lead are spaced and separated from one another outside the insulative housing, and the terminal and the lead are electrically connected to one another inside the insulative housing and outside the chip.

112. The device of claim 111, wherein the insulative housing consists of a first single-piece housing portion that contacts the lower surface and the lead and is spaced from the terminal and a second single-piece housing portion that contacts the first single-piece housing portion and the terminal.

113. The device of claim 112, wherein the first single-piece housing portion provides the top surface, the side surface and a peripheral portion of the bottom surface, and the second single-piece housing portion provides a central portion of the bottom surface within the peripheral portion of the bottom surface.

114. The device of claim 113, wherein the peripheral portion of the bottom surface is outside a periphery of the chip, and the central portion of the bottom surface is within and outside the periphery of the chip.

115. The device of claim 112, wherein the first single-piece housing portion is a transfer molded material, and the second single-piece housing portion is not a transfer molded material.

116. The device of claim 112, wherein the second single-piece housing portion includes first and second opposing surfaces, the first surface contacts the lead and the second surface provides a portion of the bottom surface.

117. The device of claim 111, wherein the terminal is within a periphery of the chip and outside a periphery of the pad, and the lead is outside the periphery of the chip.

118. The device of claim 111, wherein the terminal is integral with a planar routing line that overlaps the lead and the pad and contacts the lead inside the insulative housing, outside a periphery of the terminal and outside a periphery of the chip.

119. The device of claim 111, wherein the device includes a plurality of terminals and leads, the chip includes a plurality of pads, each of the terminals are electrically connected to one of the leads and one of the pads inside the insulative housing and outside the chip, the terminals are arranged as an array that protrudes downwardly from and extends through the bottom surface, and the leads are arranged as TSOP leads that protrude laterally from and extend through the side surface and an opposing peripheral side surface of the insulative housing.

120. The device of claim 111, wherein the device is devoid of wire bonds, TAB leads and solder joints.